SIMULATION AND COMPARISON OF NANOSCALE CMOS INVERTER IN DIFFERENT TECHNOLOGIES

Bikshalu Kalagadda[1] , Muthyala Nakshatra[2] and Keerti Kumar Korlapati[3]

[1]Department of ECE, KUCE&T, Kakatiya University, Warangal, India
[2]Department of ECE, KUCE&T, Kakatiya University, Warangal, India
[3] Department of ECE , NIT Warangal, India

ABSTRACT

The digital circuit design has two important considerations which are area and power. The design of low power devices and their implementation have got a vital role in the field of nanoelectronics. The paper analyzes the CMOS technology in the region of nanometer where the channel lengths are in nanometers like 32 nm, 45nm, and 65nm. The power dissipation of CMOS inverter is calculated. The simulation is done at various channel lengths using CMOS technology with the help of nano CMOS tool. The results are calculated at various supply voltages keeping load capacitance a constant value.

KEYWORDS

nano CMOS, nanoelectronics, low power devices, power dissipation

1. INTRODUCTION

The increasing demand for portable electronic appliances results numerous research efforts in low power VLSI circuit design. Also the need to limit the power consumption in very high density VLSI chips has led to development in low power devices. The electronic system which is powered with batteries is restricted by limited battery backup time. Due to the improvement that is taking place in scaling of MOS transistors, more number of transistors is packed into a single chip. The integration capacity of VLSI chips causes scaling in size of MOS transistors with it increasing packaging density. As the integration capacity in a chip increases it also increases the functionality and processing capacity of a chip. Due to this power dissipation may increased in VLSI chip. The CMOS technology has emerged as a vital technology in the field of nanoelectronics. There is rapid increase seen in the demand of high performance and low power devices because of technology compactness [1]-[2].

The digital market has been rapidly occupied by CMOS technologies. CMOS gates dissipated power only during switching and it requires very few devices. The dimension of MOS devices is easily scaled down when compared to others types of transistors. Also CMOS circuits have a fabrication cost at lower rates. The low cost of fabrication and also due to the placement of analog and digital circuits on the same chip uses CMOS technology. This also improves overall performance and also the packing cost is reduced [3]. In both steady state operating points as the CMOS inverter doesn't draw any current from the power source, the DC power dissipation of the circuit is neglected. The need for reducing power dissipation in electronic systems varies from application to application. The main objective in reducing the power dissipation is due to overall system cost reduction. The system cost includes system cooling cost, cost due to expensive packing technique and high electricity bill [4].

DOI : 10.14810/ijamse.2016.5104

These different requirements for reducing the overall power dissipation is attained through the proper research in designing efficient and effective low power device design. In VLSI circuit design the power dissipation is considered as issue the power dissipation is mainly due to two reasons. One is dynamic or switching power dissipation and leakage or static power dissipation. The dynamic or switching power dissipation occurs mainly due to charging and discharging of internal capacitances in the circuit [5].

The drain current which flows through NMOS and PMOS transistors in both the cases is limited to the reverse leakage current of the source and drain pn-junction. The high density chip in MOS VLSI technology design needs the packaging density of MOSFETs used in the circuits is very high. This results in the transistors size reduction as small as possible. The dimension of MOSFETs is reduced that is reduction of size which is called as scaling. The electrical properties of the MOSFET are changed because of scaling [6]. This also reduces the complexity in the circuit design. In enhancing the MOSFET characteristics, the scaling plays an important role. This also leads to further low power dissipation and also cost reduction.

Power consumption is acting as the driving force behind the changes that are occurring in the transistor technology of the interest so as design integrated circuits (IC's). The technology improvement from bipolar to NMOS and further improvement from NMOS to CMOS technologies occurred only because of the reduced power consumption [7]. The dimensions of the transistors are scaled down for the limitations of power dissipation. The power delivered is proportional to the square of supply voltage VDD power dissipation occurs due to charging and discharging of load capacitance. The expression for the power that is been delivered is given below in terms of supply voltage and other parameters [8]-[9].

$$P = C_L V_{DD}^2 F_D$$

Where P is power dissipation

C_L is load capacitance

V_{DD} is power supply and

F_D is frequency

The integrated circuits are built on CMOS devices with minimum feature sizes in nanometer. The CMOS inverter design is done at various channel lengths of 32 nm, 45nm and 65 nm using nano CMOS.

2. CMOS INVERTER AT NANO SCALE

The CMOS inverter consists of PMOS and NMOS circuits and a load capacitor which is maintained at constant value. To reduce the complexity, MOSFETs are scaled down to smaller dimensions continuously. The PMOS and NMOS devices are dealt with different channel lengths in nanometers those are 32nm, 45nm, and 60nm. The power dissipation of any MOSFET is due to leakage or static power dissipation and dynamic or switching power dissipation. In OFF-state, the main components of leakage currents are sub-threshold leakage (Isub), gate induced drain leakage (IGIDL), gate tunneling leakage (IGATE) and band-to-band tunneling (IBTBT).

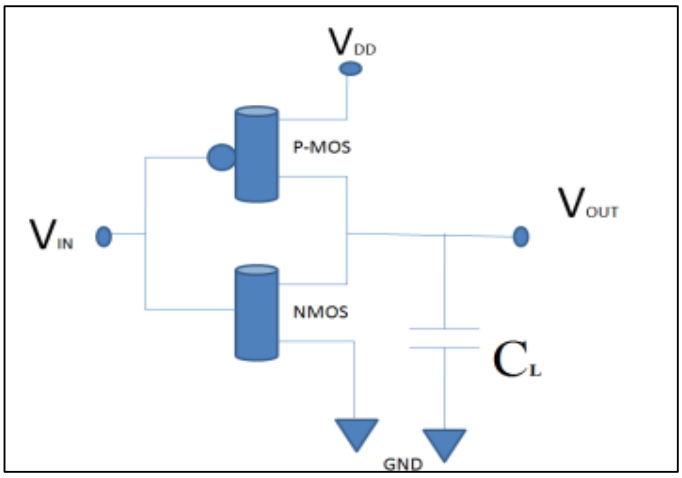

Fig. 1 CMOS inverter

The dynamic power dissipation is due to the charging and discharging of load and parasitic capacitors. Dynamic power dissipation indicate that the average dynamic power due to load capacitance.

$$P_{dynamic} = \alpha.C_L.V_{DD}^2.f + \sum_{i=1}^{n} \alpha_i.C_i.V_{DD}.(V_{DD} - V_T)$$

The dynamic power formula indicate that the average dynamic power of a complex gate due to the output load capacitance. The expression C_L indicates load capacitance, V_{DD} indicates supply voltage, f is operating clock frequency, α is switching activity of gate.

3. RESULTS AND DISCUSSIONS

The following are the simulations of PMOS and NMOS characteristics which are the circuit elements of CMOS inverter with constant load capacitance. The characteristics are estimated in different nanometer channel lengths using nanoCMOS tool.

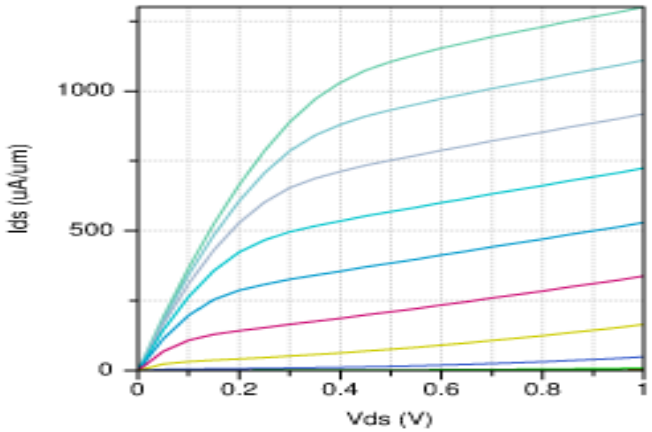

Fig. 2 NMOS characteristic in 45nm technology

The Fig. 2 above indicates the NMOS characteristics in 45nm technology. The plot of Vds drain to source voltage and Ids drain to source current is done. The simulations are done for various Vgs gate to source voltage values. The different colors indicate different values of Vgs.

The Fig. 3 indicates the PMOS characteristics in 45nm technology. The plot of Vds drain to source voltage and Ids drain to source current is done. The simulations are done here in the same way that is for various Vgs gate to source voltage values. This Figure mainly explains how the ptype MOSFET varies from other types.

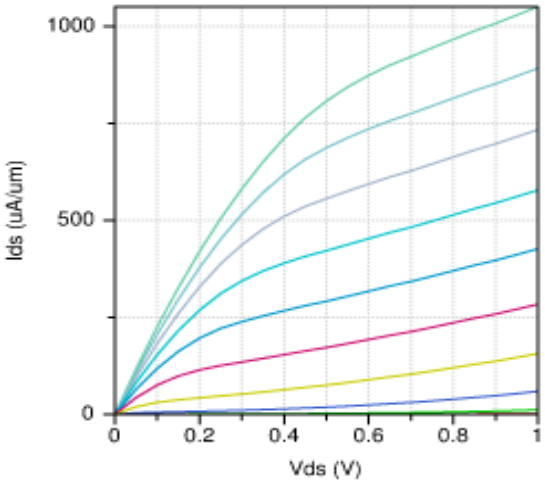

Fig. 3 PMOS characteristic in 45nm technology

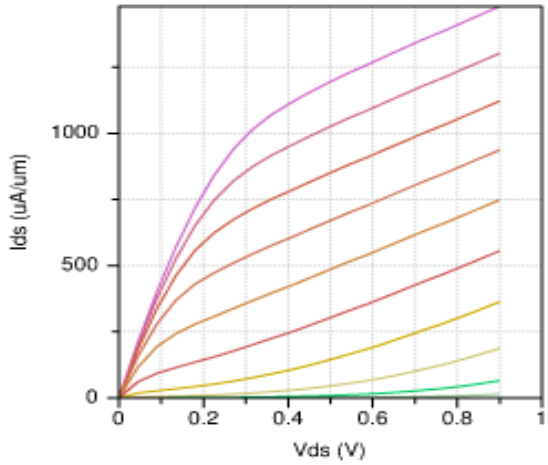

Fig. 4 NMOS characteristic in 32nm technology

The Fig. 4 indicates the NMOS characteristics in 32nm technology. The plot of Vds drain to source voltage and Ids drain to source current is done. The simulations are done here in the similar manner done above. Similarly the above Figures are used to show the simulation results by their characteristic graph for either NMOS or PMOS in various technologies i.e., 32 nm and 65 nm technologies.

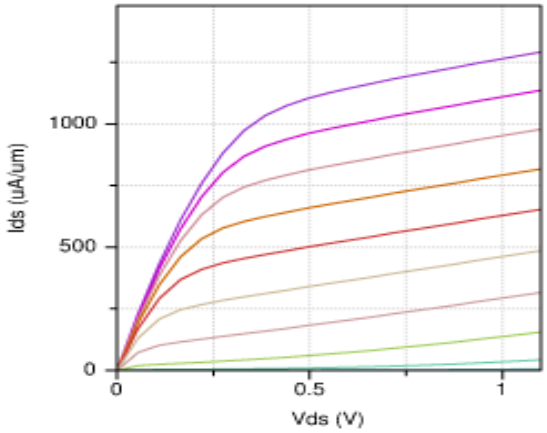

Fig. 5 NMOS characteristic in 65nm technology

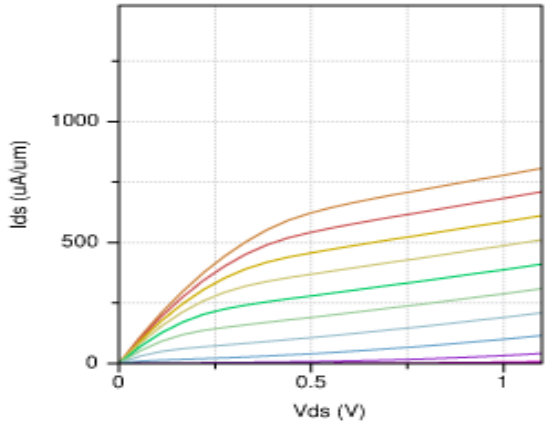

Fig. 6 PMOS characteristic in 65nm technology

Table1. Average power dissipated with channel length

Channel Length (nm)	Optimum Supply Voltage (v)	Power dissipation (NanoWatts)
65nm	1.5	432
45nm	1.1	398
32nm	0.95	24106

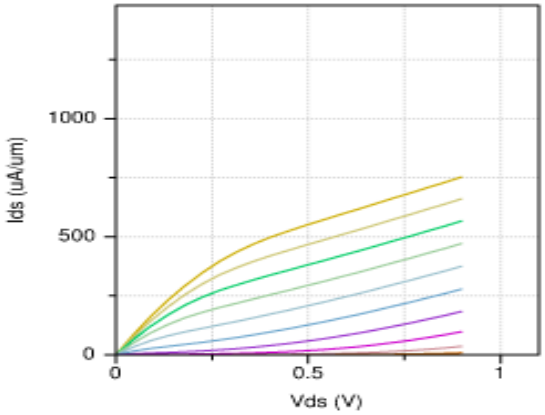

Fig. 7 PMOS characteristic in 32nm technology

4. CONCLUSION

The simulated characteristics above depict how CMOS inverter operates at various technologies of whose channel lengths are in nanometers. The variation of voltages input and output help us to find out the average power dissipated at various channel length in accordance with the different power supply. The table above shows the average power dissipated in accordance with channel length. As the channel length is reduced, the power dissipation values are changed. The inverter characteristics are studied at constant load capacitance value. The performance of PMOS and NMOS at different channel lengths is observed. It is known that when PMOS is active, NMOS is in cutoff condition and vice versa. Accordingly they output the voltages of their conditions. This work can be further extended by still reducing the channel lengths in nanometer region

REFERENCES

[1] Sung-MO (Steve) Kang, Yusuf leblebici- 3rd edition CMOS Digital Integrated Circuits: Analysis and Design.

[2] Sylvester, Senior Member IEEE, and Ashish Srivastava, Member IEEE; Computer-Aided Design for LowPowerRobust Computing in Nanoscale CMOS.

[3] Yangang Wang, Michael Merrett and Mark Zwolinski, Statistical Power Analysis for Nanoscale CMOS

[4] N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design:A Systems Perspective. Reading, MA: Addison-Wesley, 1993

[5] Hon Sum Philip Wong, David J. Frank, Paul M. Solomon, Clementh J. Wann, & Jeffrey J. Welser, Nanoscale CMOS; PROCEEDINGS OF THE IEEE, VOL. 87, NO. 4, APRIL 1999

[6] T. Ghani et al., ―A 90-nm high volume manufacturing logic technology featuring novel 45-nm gate length strained silicon CMOS transistors, in IEDM Tech. Dig., 2003, pp. 978–980.

[7] Silvaco Int., Santa Clara, CA, 2010 ATLAS User's Manual A 2-D Numerical Device Simulator.

[8] Alexei Nazarow, J.P. Colinge et al (2011). Semiconductor on InsulatorMaterial for Nanoelectronics Applications, Springer Heidelberg Dordrecht, London.

[9] R. Chau, et al., International Conference on Solid State Devices & Materials, Nagoya, Japan, 2002, pp. 68–69.

Authors

Bikshalu Kalagadda was born in 1980. He received his B.Tech, M.Tech and Ph.D from jawaharlal Nehru Technological University Hyderabad in 2002, 2007 and 2015 respectively. Currently he is working as an Assistant professor in the Department of Electronics and Communication Engineering, Kakatiya University Warangal. His current research interests include Nano electronics and nano devices for future technologies.

Muthyala Nakshatra received her B.Tech from KU College of Engineering and Technology in 2013. At present she is pursuing M.Tech in KU College of Engineering and Technology in the Department of Electronics and Communication Engineering. Her research interests include image processing and nanoelectronics.

Keerti Kumar K was born in 1985. He received his B.Tech degree from Jawaharlal Nehru Technological University, Hyderabad in 2006. He received his M.E degree from Osmania University, Hyderabad in 2008. Currently he is working towards his Ph.D degree from National Institute of Technology Warangal. His current research interests include Device Modeling, Nano scale semiconductor devices, Nano biomedical electronic sensors and MEMS.