EFFECT OF MESH GRID STRUCTURE IN REDUCING "HOT CARRIER EFFECT" OF NMOS DEVICE SIMULATION

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ABSTRACT

This paper presents the critical effect of mesh grid that should be considered during process and device simulation using modern TCAD tools in order to develop and optimize their accurate electrical characteristics. Here, the computational modelling process of developing the NMOS device structure is performed in Athena and Atlas. The effect of Mesh grid on net doping profile, n++, and LDD sheet resistance that could link to unwanted "Hot Carrier Effect" were investigated by varying the device grid resolution in both directions. It is found that y-grid give more profound effect in the doping concentration, the junction depth formation and the value of threshold voltage during simulation. Optimized mesh grid is obtained and tested for more accurate and faster simulation. Process parameter (such as oxide thicknesses and Sheet resistance) as well as Device Parameter (such as linear gain "beta" and SPICE level 3 mobility roll-off parameter " Theta") are extracted and investigated for further different applications.

KEYWORDS

Hot Carrier Effect(HCE), Technology Computer Aided Design(TCAD), N-Channel MOS (NMOS).

1. INTRODUCTION

Hot carriers are either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities (near the drain) within a semiconductor MOS device. They are injected into the oxide with enough energy to create defect states (traps) in the oxide near the silicon/oxide interface [1] where they shouldn't be, forming a space charge that causes the device to degrade or become unstable. The term 'hot carrier effects', therefore, refers to device degradation or instability caused by hot carrier injection.

High field induced hot-carrier (HC) degradation affects reliability and causes long-term instability [2][3], manifested by a threshold voltage increase and drive current reduction. It is found that only hot electrons having energy of 0.6eV larger than the Si-SiO2 conduction band discontinuity can cause SiO2 degradation in n-channel MOSFETs. The degradation is attributed to the breaking of the ≡SiH bond at the interface [1][4]. Because of their high kinetic energy, hot carriers can even get injected and trapped in areas of the device where they shouldn't be, forming a space charge that causes the device to degrade or become unstable. The term 'hot carrier effects', therefore, refers to device degradation or instability caused by hot carrier injection. Studies have

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shown that the worst effects occur when VD = 2VG. These trapped charges shift some of the characteristics of the device, such as its threshold voltage (Vth) and its conveyed conductance (gm).

Thus, optimum design of devices to minimize, if not prevent, hot carrier effects is the best solution for hot carrier problems. Common design techniques for preventing hot carrier effects include: 1) increase in channel lengths; 2) n+ / n- double diffusion of sources and drains; 3) use of graded drain junctions; 4) introduction of self-aligned n- regions between the channel and the n+ junctions to create an offset gate; and 5) use of buried p+ channels. If we want to simulate the optimal design of NMOS without HCE, all these techniques need a near perfect mesh grid design with less computational time. We therefore proposed in this paper the study and optimal design of this mesh grid using one of the standard TCAD tool Silvaco ATHENA and ATLAS.

2. MATHEMATICAL MODEL

Various models are used to describe HC degradation, of which the most widely adopted is the 'lucky electron' model, proposed by Shockley [5]. It is based on the assumption that only the hot electrons accelerated by the electric field and not suffering collisions are most likely to cause impact ionization. The probability of an electron obtaining enough energy Eb to surmount oxide barrier, given an electric field E is [3][6] of the form PEb =exp(−Eb/qEl). The probability of a hot electron travelling a distance d arriving at the interface Si/SiO2 without suffering from energy loss collisions is [7] of the form Pd = exp(−d/ l) , where l is the hot electron mean free path. Consequently, the injection probability is proportional to the product of these two probabilities [8][9],

$$Ig=C_1 I_d P_{Eb} P_d$$

where C_1 is a fitting coefficient and I_d is the drain current.

Performance degradation can become severe at elevated temperatures even at low fields. Negative bias temperature instability (NBTI) is another very important reliability concern for contemporary p-channel MOSFETs. The threshold voltage shift primarily depends on stress bias condition, stress time and stress temperature. The observed power-law dependence on stress time [10][11] is explained by the Si-SiO2 interface diffusion-reaction model [4]. This can be used to estimate the threshold voltage shift due to NBTI [12], where Ea is a fitting parameter (the NBTI activation energy) and C2 and γ are fitting coefficients.

The wide use of nitrogen in sub-2nm gate oxides is found to enhance NBTI [13]. NO gas annealing leads to lower activation energy Ea and nitride oxides acquire more positively charged traps during stress compared to the pure SiO2, which degrades the transistor lifetime by 2 to 3 decades. From a device design point of view, the suppression of the impact of nitrogen on NBTI is an important concern. It is worth noting that the NBTI degradation is recoverable. While static measurement of NBTI shows continuous degradation, pMOSFETs under dynamic stress conditions undergo passivation/relaxation stages between stresses, and the threshold voltage accordingly recovers after stress removal [14][15].

Greater HC degradation is observed in narrow-width MOSFETs with STI [16], although initial impact ionization rate is not bigger than that of large channel width fresh devices. This effect is ascribed to the increase of impact ionization rate and injection rate in narrow n-MOSFETs [16] and a higher oxide electron trapping efficiency in narrow p-MOSFETs [17].

3. NMOS DEVICE SIMULATION

3.1. Methodology

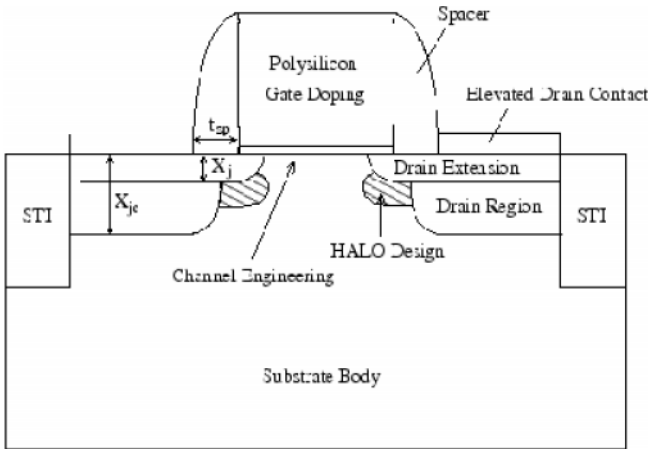

Figure 1 .Schematic model of the proposed NMOS device

ATHENA predicts the physical structures that result from processing steps. The resulting physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions. ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes.

By applying a set of differential equations, derived from Maxwells laws, onto this grid we can simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modelled in DC, AC or transient modes of operation. The Maxwell Laws can be summarized as:

a) Divergence of electric flux from the control volume = Charge Density in the control volume (Poisson's Equation) or Divergence of electric flux = zero (Laplace's Equation);

b) Divergence of electrons from a control volume = difference in generation rate and recombination rate of electrons in the control volume;

c) Divergence of holes from a control volume = difference in generation rate and recombination rate of holes in the control volume;

d) Total electron current density = drift electron flux density + diffusion electron flux density;

e) Total hole current density = drift hole flux density + diffusion hole flux density;
First three are coupled; non-linear second order partial differential equations and last two are transport equations. Solution of these five equations gives the simulated predictions.
The intersections of the grid lines give the nodes. As shown in Fig.2(b), At node (i,j) there are three unknowns vij , nij and pij .Initial intelligent guess is made of vij , nij and pij . Using these values we solve the Poisson equations and the continuity equations for electron and holes until we get converging results.

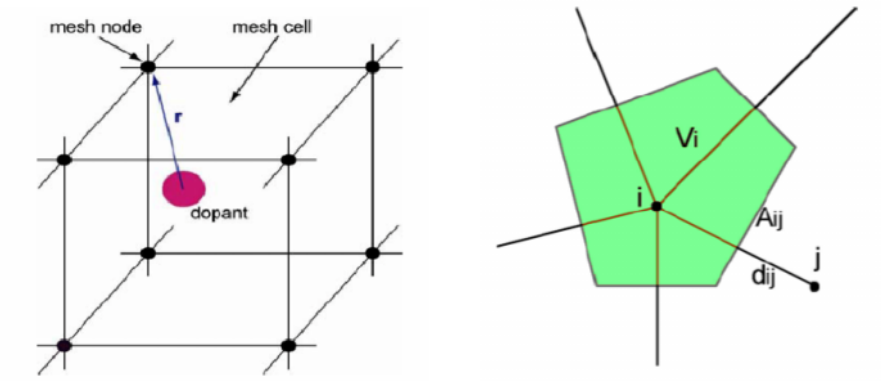

Figure 2 (a). Schematic view of a mesh cell containing a discrete dopant. The point charge of dopant is assigned to those neighbouring nodes according to various charge assignment schemes. **(b)** Schematic view of box discretization method in 2D. Vi is the box volume associated with grid i, Aij is the interface area between boxes of i and j, and dij is the distance between i and j.

3.2. Transport equations

The governing equations of semiconductor carrier transport include the Poisson equation and electron and hole continuity equations. The Poisson equation derives from Maxwell's equations and can be written in the form

$$\nabla.(-\varepsilon\nabla\phi) = \rho = q(p - n + N_d^+ - N_a^-) + \rho_{trap}$$

where ε is the permittivity; φ is the electrostatic potential; ρ is the charge density, q is the elementary electronic charge; n and p are electron and hole concentration; d N+ and a N− are the ionized donor and acceptor concentrations; and ρ trap is the trap and fixed charge density.
The Poisson equation is solved self-consistently with the current continuity equations for electrons and holes.

$$\nabla.\overline{J_n} = q(R_{net} + \frac{\partial_n}{\partial_t}),$$

$$\nabla.\overline{J_p} = -q(R_{net} + \frac{\partial_p}{\partial_t})$$

which are deduced from $\nabla \cdot J + \partial p / \partial t = 0$ obtained from Ampere's circuital law. In equations, Jn and Jp are current densities for electrons and holes and Rnet is the net electron hole recombination rate.

Depending on the complexity of semiconductor structure and the carrier transport behavior, different transport models can be chosen, usually based on various approximations to the full Boltzmann transport equation. Models describe the current density with different degrees of complexity and may include self-heating and carrier energy transport. The Drift-diffusion model is one of the simplest approaches. It describes the current as a sum of two components describing the drift of carriers under the influence of the electric field and diffusion driven by concentration gradients.

$$\overrightarrow{J_n} = qD_n\nabla n - q\mu_n n\nabla\phi = -qn\mu_n\nabla\phi_n$$

$$\overrightarrow{J_p} = qD_p \nabla p - q\mu_p p \nabla \phi = -qp\mu_p \nabla \phi_p$$

where μn and μp is the electron and hole mobility; D is the diffusion coefficient which obeys Einstein relation when the system is close to thermal equilibrium namely D = μ kT/q. Φn and Φp are electron and hole quasi-Fermi potentials described as,

$$\phi_n = \phi_i - \frac{kT}{q} \ln\left(\frac{n}{n_i}\right)$$

$$\phi_p = \phi_i + \frac{kT}{q} \ln\left(\frac{p}{n_i}\right)$$

Where ni is the intrinsic electron density, and φi = − Ei/ q is the electrostatic potential defined in terms of the intrinsic Fermi level Ei..

3.3. Numerical methods of TCAD

Numerical methods are used to obtain solutions of the semiconductor equations described in the previous section for devices with realistic geometries and doping concentrations. The equations are discretised over a mesh or grid covering the device simulation domain using finite difference or finite element techniques, resulting in large system of algebraic equations. In the case of the box integration approach, which is a modification of the finite element approach, Gauss's theorem is used to transform the governing equations into the following integral form

$$\varepsilon \int_{\partial v} \nabla \phi \cdot dA + \int_v \rho dV = 0$$

$$\int_v \left(\frac{\partial n}{\partial t} + R_{net}\right) dV - \frac{1}{q} \int_{\partial v} \overrightarrow{J_n} \cdot dA = 0$$

$$\int_v \left(\frac{\partial n}{\partial t} + R_{net}\right) dV + \frac{1}{q} \int_{\partial v} \overrightarrow{J_n} \cdot dA = 0$$

The current densities are similarly discretised according to the neighbour grids. A single box in the mesh for the set of discretized equations is shown in Fig.2(a).

The set of algebraic equations obtained is nonlinear, and Newton or Gummel procedures are used for their linearization. The Gummel iteration method is well known for its stability There are two methods for solving for these three unknowns: Coupled Method and Uncoupled Method or Sequential Method. There are three advantages of physically-based simulation. It is predictive, it provides insight, and it conveniently captures and visualizes theoretical knowledge. Physically-based simulation is different from empirical modelling. The goal of empirical modelling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge.

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure.The drawbacks of physically-based simulation are that all the relevant physics must be incorporated into a simulator, and numerical procedures must be

implemented to solve the associated equations. These tasks have been taken care of for users of ATLAS.Those who use physically-based device simulation tools must specify the problem to be simulated. In ATLAS, specify device simulation problems by defining:

• The physical structure to be simulated.
• The physical models to be used.
• The bias conditions for which electrical characteristics are to be simulated. An important point to remember when using Technology Computer Aided Design (TCAD) is that the most critical task is to accurately model the process flow.

For accurate MOSFET simulation, we should invest 90% of the time in achieving an accurate process simulation, while only investing 10% of the time in fine-tuning the device simulation.
The reason for this, especially for silicon technologies, is that the device physics, in general, is understood. For silicon, not only is the physics well understood, it is also well characterized, so most of the default values in ATLAS will be correct. Therefore, the calibration of an ATHENA process file does not involve the calibration of well known quantities such as diffusion coefficients. Instead, the calibration involves variables that are process and production line dependent. For example, the damage caused by an implant cannot be determined exactly, since it is dose rate dependent and can be influenced by beam heating of the substrate, which is dependent on the carousel rotation speed and the efficiency of the cooling system.

3.4. TCAD Simulation

Typical NMOS fabrication process steps are chosen from reference [19]. Structure of NMOS is created based on half NMOS and structure manipulation is the process of reflecting the half NMOS to have a full NMOS device. If the process has been correctly modelled, the device simulation will also be accurate if appropriate models have been chosen. If a simulated device exhibits electrical characteristics that are totally inaccurate, we may have done something wrong in the process simulation.

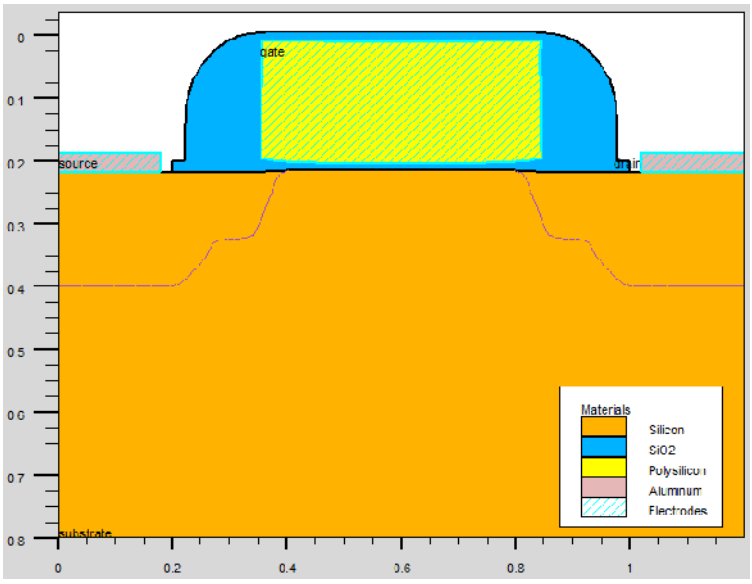

Figure 3 Simulated NMOS model

The first important point is to ensure that we let the device simulator calculate the work function of the gate electrode from the simulated doping profile rather than assigning a value to it. This

means, making sure that the polysilicon gate is not itself defined as an electrode but rather a layer of metal, usually aluminium, is deposited on top of the polysilicon gate. Therefore, this metal layer is the film defined as the electrode. The effective work function of the poly gate will then be correctly calculated from the doping profile in the polysilicon.

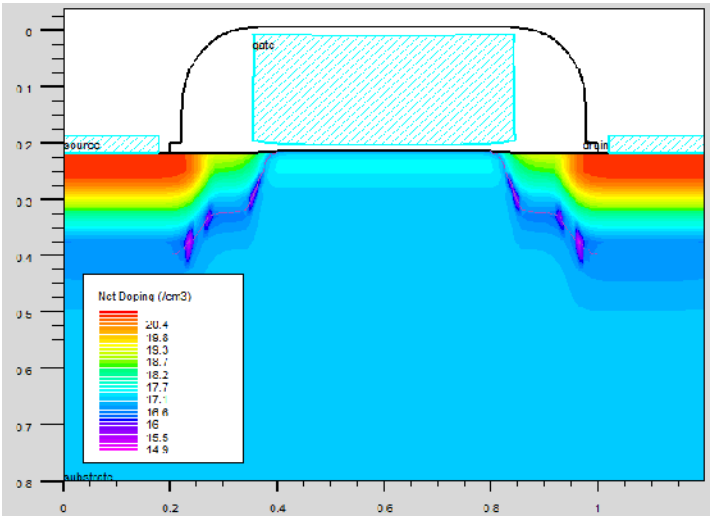

Figure 4 Net Doping profile in the model

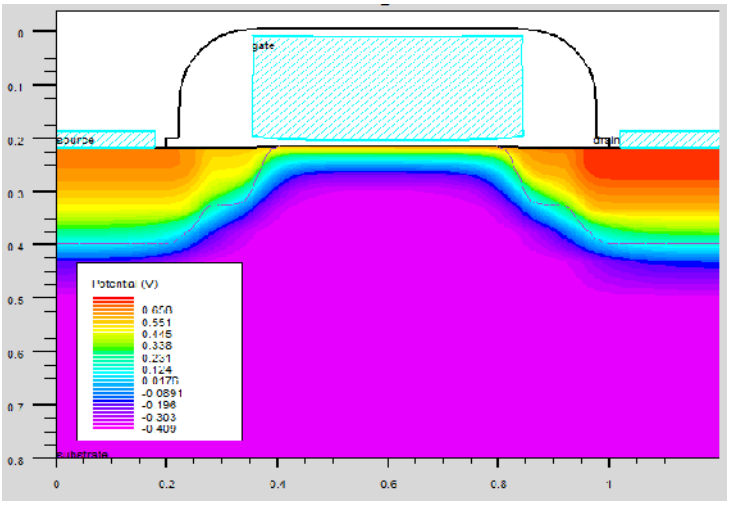

Figure 5 Potential Profile developed in the model

An important area for accuracy in MOSFETs is modelling the inversion region under the gate. As it is, this charge that is responsible for current conduction in the device. The inversion region charge under the gate-only extends approximately 30 Angstroms into the silicon. The inversion region charge density under the gate falls off rapidly with depth into the silicon. It is imperative that there are several mesh points in the Y direction in this inversion region to model the drain current correctly. Accordingly, we recommend that the mesh spacing under the gate be no more than 10 Angstroms (1 nm).

We think that a 10 Angstrom mesh under the gate would result in a huge number of mesh points. But, there only needs to be approximately three mesh points within the inversion region in the Y direction. The grid spacing can increase rapidly in spacing away from the oxide-silicon interface.

The simulated NMOS model of GRID1 is shown in Fig.3 along with corresponding Net doping Profile in Fig.4 and potential profile in Fig.5.

4. RESULT AND DISCUSSION

We select the grid spacing given in Table 1 for our modelling and device optimization based on previous standard model obtained from various recent published literatures. Both Fig. 6 and Fig.7 shows the effects of changing the mesh spacing at the interface on the simulated drain current. We can see from this figure that too coarse of a mesh always results in too high of a current simulated. The mesh grid effects to net doping is again observed by the relationship off the n++ and LDD sheet resistance in Fig.8. The optimization of the NMOS device was done systematically by changing individual process parameters laid out by the ATHENA example [20] and the resulting characteristics were studied. Like the channel doping, the type of atom being implanted, the dosage and the energy of the implant all effect the resulting doping concentration and depth of the implanted ions. Again the dosage can be modified to produce varying doping concentrations in the light drain/source. An increase in the light drain/source doping greatly increased the transconductance but had no affect on the threshold voltage.

Table 1 Six different GRID spacing needed for optimisation

GRID1	line y loc=0.2 spac=**0.005** line y loc=0.5 spac=0.05
GRID2	line y loc=0.2 spac=**0.010** line y loc=0.5 spac=0.05
GRID3	line y loc=0.2 spac=**0.020** line y loc=0.5 spac=0.05
GRID4	line y loc=0.2 spac=**0.040** line y loc=0.5 spac=0.05
GRID5	line y loc=0.2 spac=**0.080** line y loc=0.5 spac=0.05
GRID6	line y loc=0.2 spac=**0.160** line y loc=0.5 spac=0.05

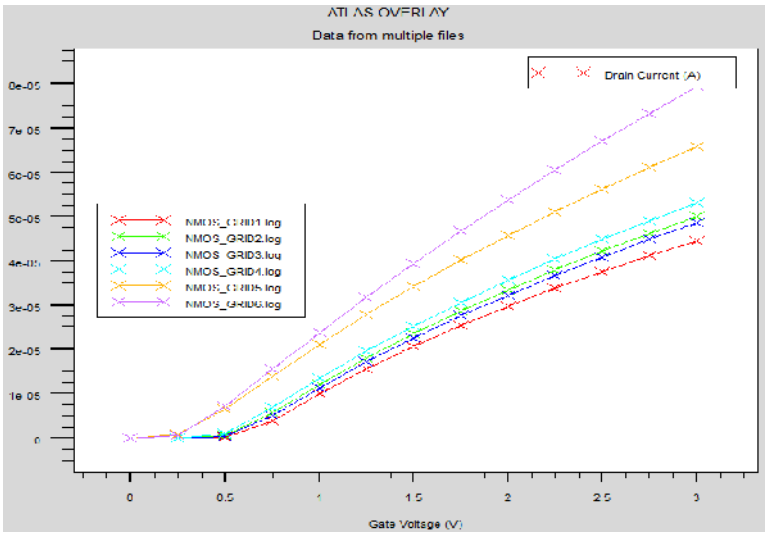

Figure 6 The effect of grid changes in y-axis to transfer characteristic graph (Id-Vg plot)

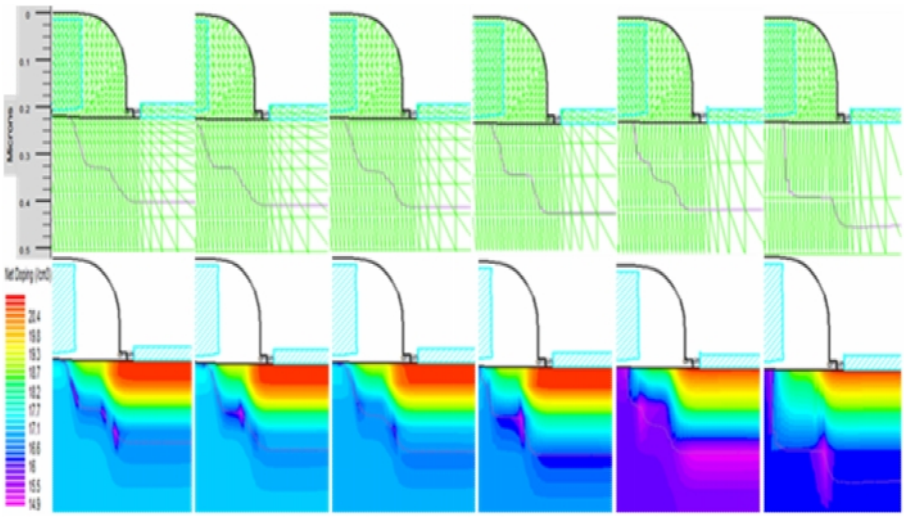

Figure 7 The effect of grid changes in y-axis to Net doping of the device [GRID1, GRID2, GRID3, GRID4 ,GRID5 ,GRID6]

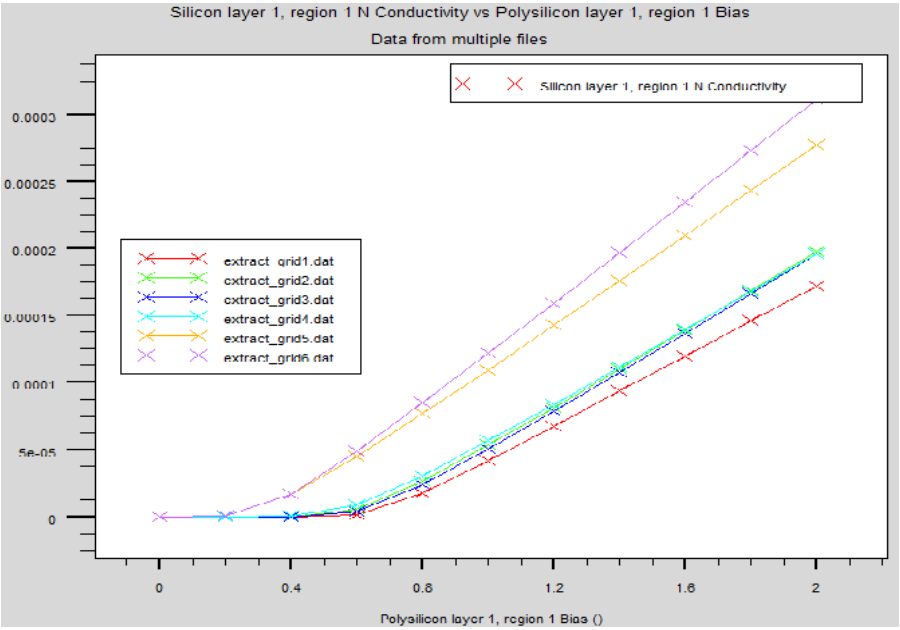

Figure 8 The effect of grid changes in y-axis to conductivity of polysilicon layer (LDD sheet resistance graph)

Table 2 The overall affect of the process parameters [18-19]

	Threshold Voltage	Transconductance
Increasing Mesh Grid density	INCREASE	DECREASE
Increasing Gate Oxide Thickness	INCREASE	DECREASE
Increasing Channel Doping	INCREASE	NO CHANGE
Increasing light d/s doping	NO CHANGE	INCREASE
Increasing Heavy D/S Doping	NO CHANGE	INCREASE

Table 2 is used to compile the affects of each process parameter on the threshold voltage and transconductance. The knowledge of these affects provides the means to optimize the NMOS transistor to the desired characteristics. Fig. 9 also reveals the increased transconductance and lower threshold voltage of the optimized device compared to the initial example. The optimized device will provide a much higher switching speed (lower propagation delay) in the CMOS digital logic inverter application over the original device.

Moreover, as we mentioned earlier that the doping concentration and depth of the implanted ions (i.e. total net doping) is found to be greatly affected by the resolution of the device mesh grid as seen in Fig. 7. And the optimal net doping design for LDD/graded drain junction NMOS is one of the method to minimize Hot Carrier Effect. And in our optimal design, Hot Carrier Effect (HCE) is found to be drastically reduced with the selecting of proper grid spacing/net doping indicated by the reduction of threshold voltage and the increase in transconductance as seen in Fig.9 as compared to the reference original model[20].Some important input parameters and extracted output parameters are given in Table 3 and Table 4 respectively.

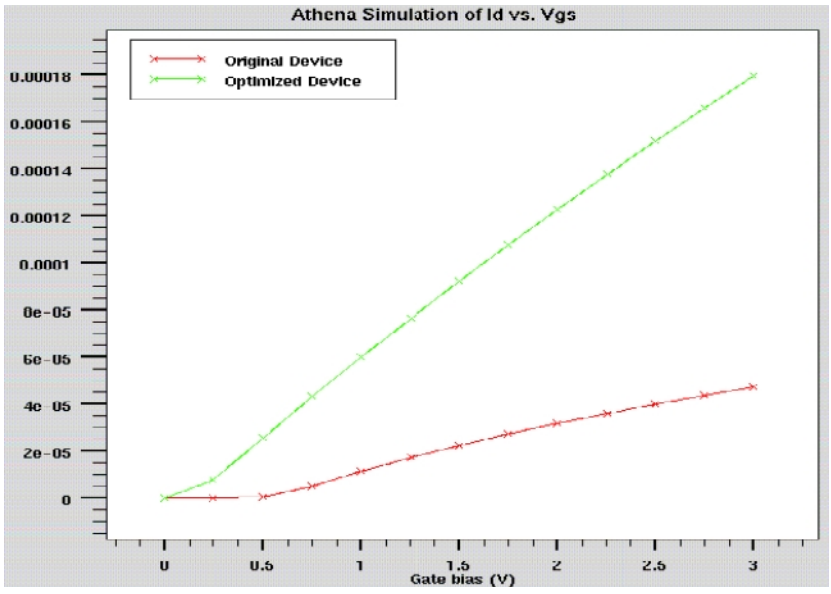

Figure 9 Original versus optimized device characteristics

5. CONCLUSIONS

It is found that the Mesh grid parameter could give profound effect to the simulation process of NMOS device. More coarser grid such as Grid 5 and Grid 6 have lower threshold voltage but higher values of saturation currents while finer Grid 1, Grid 2, Grid 3 and Grid 4 have higher threshold voltage with lower saturation current. Through our observations, Grid 2 and Grid 3 which is much denser and consumes longer time to complete simulation compare to Grid 4 is not necessary to be used since Grid 4 will provide almost similar result. Again Grid 4 has lower threshold voltage and good transconductance than other Grid configuration. Grid 4 therefore should have minimum Hot Carrier Effect with acceptable net doping profile. It can be concluded that the correct specification of grid is critical in process and device simulation. The number of nodes in the grid has a direct influence on simulation accuracy and time. A finer grid should exist in those areas of the simulation structure where ion implantation will occur to reduce HCE and where p-n junction will formed to have accurate active region. And this net doping changes due to mesh grid are more significant as y-axis changes compared with variation in x-axis grids.

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APPENDIX

Table 3 Important constant parameters used in the design

Boltzmann's constant	1.38066e-023 J/K
Elementary charge	1.60219e-019 C
Permittivity in vacuum	8.85419e-014 F/cm
Temperature	300 K
Thermal voltage	0.025852 V
Epsilon	11.8
Eg (eV)	1.08
Chi (eV)	4.17
Nc (per cc)	2.8e+019
Nv (per cc)	1.04e+019
ni (per cc)	1.45e+010

Table 4 Extracted device parameters from the optimal model

n++ sheet rho	29.0937 ohm/square
ldd sheet rho	2176.85 ohm/square
chan surf conc	3.73448e+016 atoms/cm3
long channel Vt (n1dvt)	0.610618 V
Nvt	0.534383
Nbeta	0.00023928
Ntheta	0.131034

ATHENA AND ATLAS CODE

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.2 spac=0.006
line x loc=0.4 spac=0.006
line x loc=0.6 spac=0.01
line y loc=0.0 spac=0.002
# spac=0.005 to 1.60 variations
line y loc=0.2 spac=0.005
line y loc=0.5 spac=0.05
line y loc=0.8 spac=0.15
init orientation=100 c.phos=1e14 space.mul=2

diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
etch oxide thick=0.02
implant boron dose=8e12 energy=100 pears
diffus temp=950 time=100 weto2 hcl=3
diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
diffus time=220 temp=1200 nitro press=1
etch oxide all
diffus time=20 temp=1000 dryo2 press=1 hcl=3
etch oxide all
diffus time=11 temp=925 dryo2 press=1.00 hcl=3
extract name="gateox" thickness oxide mat.occno=1 x.val=0.05
implant boron dose=9.5e11 energy=10 pearson
depo poly thick=0.2 divi=10
etch poly left p1.x=0.35
method fermi compress
diffuse time=3 temp=900 weto2 press=1.0
implant phosphor dose=3.0e13 energy=20 pearson
depo oxide thick=0.120 divisions=8
etch oxide dry thick=0.120
implant arsenic dose=5.0e15 energy=50 pearson
method fermi compress
diffuse time=1 temp=900 nitro press=1.0
etch oxide left p1.x=0.2
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18
   extract name="nxj" xj silicon mat.occno=1  x.val=0.1junc.occno=1
   extract name="n+ + sheet rho" sheet.res  material="Silicon" mat.occno=1 x.val=0.05 region.occno=1
extract name="ldd sheet rho" sheet.res material="Silicon" \
        mat.occno=1 x.val=0.3 region.occno=1
       extract name="chan surf conc" surf.conc impurity="Net  Doping" \
        material="Silicon" mat.occno=1 x.val=0.45
extract start material="Polysilicon" mat.occno=1 \
bias=0.0 bias.step=0.2 bias.stop=2 x.val=0.45
extract done name="sheet cond v bias" \
   curve(bias,1dn.conduct material="Silicon" mat.occno=1  region.occno=1)\
        outfile="extract1.dat"
extract name="n1dvt" 1dvt ntype vb=0.0 qss=1e10 x.val=0.49
structure mirror right
electrode name=gate x=0.5 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.1
electrode name=substrate backside
structure outfile=NMOS_GRID1.str
tonyplot  NMOS_GRID1.str -set nmos_nd.set
```

```
go atlas
models cvt srh print
contact name=gate n.poly
interface qf=3e10
method newton
solve init
solve vdrain=0.1
log outf=NMOS_GRID1.log master
solve vgate=0 vstep=0.25 vfinal=3.0 name=gate
save outf=NMOS_GRID1.str
tonyplot  NMOS_GRID1.log -set nmos_log.set
extract device parameters
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
      - abs(ave(v."drain"))/2.0)
extract name="nbeta" slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
      * (1.0/abs(ave(v."drain")))
extract name="ntheta" ((max(abs(v."drain")) * $"nbeta")/max(abs(i."drain"))) \
      - (1.0 / (max(abs(v."gate")) - ($"nvt")))

quit
```

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