A DESIGN GUIDE FOR COMPARATOR-BASED SWITCHED-CAPACITOR INTEGRATOR

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ABSTRACT

Comparator-Based Switched-Capacitor (CBSC) Integrator is main part of Sigma-Delta Modulators. In this paper required equations presented and Logic Part of CBSC Integrator introduced in Gate Level. The Parameters are Capacitance (C), Current (I), Comparator Delay (Td), Current Source Output Resistance (Rout) and Comparator Threshold (VCT).

KEYWORDS

CMOS, Integrator, CBSC, delay time

1. INTRODUCTION

The Comparator-Based Switched-Capacitor Circuits (CBSC) is an appropriate method to design circuits by today technology [1-13]. With OPAMP based circuits, the accuracy of the circuit is very dependent of the open loop gain of the OPAMPs [14-17]. It is possible to compensate by using cascod devices, cascading several stages, compensation techniques [16] and so on. This again causes new problems such as high power consumption and stability issues [19].

CBSC has benefits which coincide well with technology scaling. Instead of forcing the input nodes to the ground, the charge transfer process is performed by current sources, while the virtual ground condition is detected by a comparator instead of being forced by OPAMPs [1]. This makes it possible to also take advantage of the increased speed in modern technologies to create high-speed comparators. Also, stability issues are removed with absence of the OPAMP.in this paper we present the required circuits and equations for designing a CBSC integrator in section III. Section IV is about logic part of CBSC integrator that produces control signals and in section V we explain an example in order to more clearance.

2. INPUT CBSC INTEGRATOR FOR DELTA-SIGMA MODULATOR

This type of integrator is suitable for using in delta-sigma modulator (fig.1) [1].

As the first and important component in the delta-sigma modulator, the input integrator should be considered since it affected directly on the input signal, this integrator dominates the total performance of the sigma-delta modulator.

An approximation used for the total input referred integrator noise power can be derived as (1) [1]:

$$N_{in,tot} = \sum_{i=1}^{n} \frac{N_{in,i}}{\pi(2i-1)\prod_{j=1}^{i-1} a_j^2} \cdot \left(\frac{\pi}{OSR}\right)^{2i-1} \quad (1)$$

In the equation i is the i^{th} integrator, a_j are coefficients before the i^{th} integrator, N_{in} is the noise power of integrator and OSR is the oversampling ratio. This decrease input referred noise of the input integrator by 1/OSR compared to a standalone integrator, improving requirements for the analog circuitry. As an example for 2^{nd} integrator, the input referred noise is reduced by ($\pi^2 / (3a_1 \times OSR^3)$). This shows that the input integrator is very important for oversampling delta-sigma modulators [2-12].

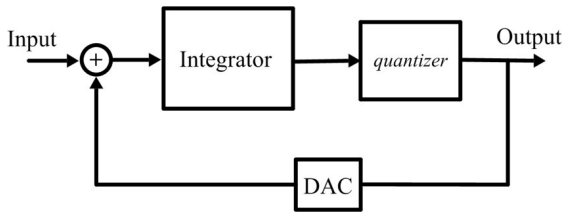

Fig.1 A general model of delta-sigma modulator

The CBSC integrator shown in Fig. 2 consists of a comparator followed by a logic unit which generates control signals such as E1 (coarse charge transfer), E2 (fine charge transfer), S (output switch), and P (preset switch). E1 and E2 are then applied to two linear current sources, I1 and I2, which charge and discharge the load capacitor as coarse and fine charge transfer, respectively. The timeline of this integrator is shown in Fig.3. During the sampling phase and according to that Figure, the input signal is sampled in *Cs* and the charge transfer phase begins with rising *Φ2*. In the beginning of this phase, a preset pulse is applied to the output, connecting it to the lowest voltage in the circuit. Then a coarse charge transfer phase E1 and a fine charge transfer phase E2 charge and discharge the load capacitor, respectively, in order to create a virtual ground effect. During the preset phase, the virtual ground node (the comparator positive input), Vx, drops below the common-mode voltage, Vcm, and thus resetting the comparator.

The logic control part raises E1, and I1 charges the load capacitor (output node) up to the virtual ground node equals to the common-mode voltage (coarse charge transfer). However, at this time, the load capacitor charge will be higher than its proper value due to the comparator delay time. So an overshoot error is produced, as shown in Fig.3. To solve this issue, the logic control part will pull down E1 and raise E2, causing a discharge of the output node by I2 (fine charge transfer) which has slower rate compared with I1, until the virtual ground node voltage becomes lower than Vx. Here, the comparator output will reset again and both E1 and E2 will be zero. Also, switch S will be opened by the logic control part and the correct value of input sampled on the load capacitor (which is the sampling capacitor of the next stage). The output is slightly lower than the ideal value because of the comparator delay time. This delay time produces at each cycle a constant signal-independent undershoot, as shown in Fig.3.

In fact, we need to reach the correct output value only at the sampling instant without having to worry about how it reaches there. By this procedure we should be able to detect the virtual ground effect in order to remove the OPAMPs. This strategy helped us to solve the issues of speed, gain,

and stability. Replacing OPAMPs with comparators has also a significant effect on power consumption due to lower power dissipation of comparators versus OPAMPs.

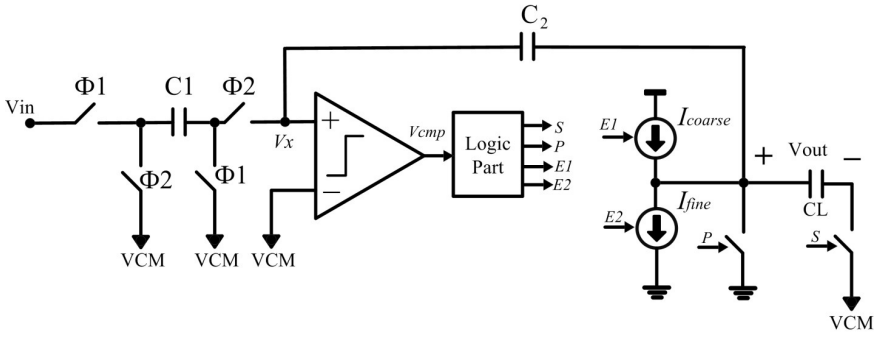

Fig.2 general schematic of CBSC Integrator

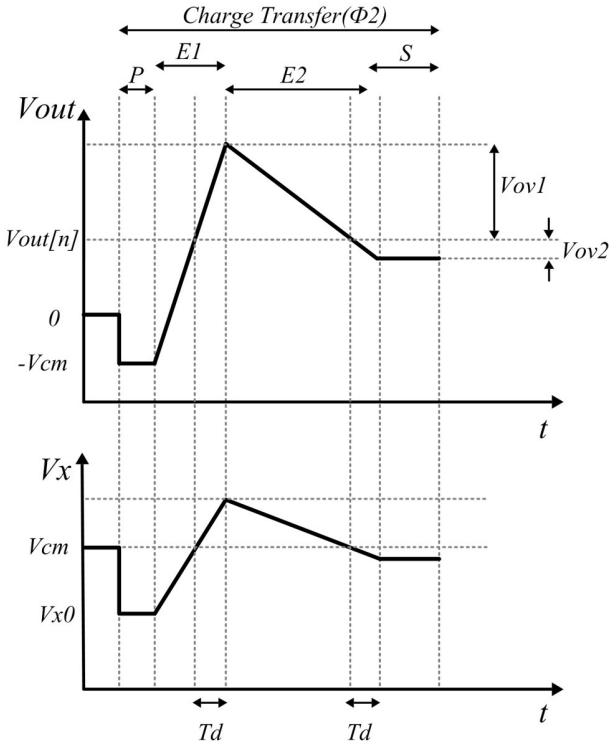

Fig.3 . timeline for Vx and Vout

3. Design equations

The required parameters for CBSC integrator are sampling and feedback capacitors (C), switch resistance, value of coarse current source (I), comparator delay (T_d), current source output resistance (R_o), and comparator threshold (V_{ct}). The most important issue that limits the Switched-Capacitor performance is thermal noise. The mean squared noise of RC equivalent circuit is equal to (2).

$$\overline{V_n^2} = \frac{k_B T}{C} \qquad (2)$$

As shown in (1), noise from the first integrator is also suppressed by 1/OSR. Thus, the total input referred thermal noise from the first differential SC integrator can be found as:

$$P_{no,diff} = \frac{2k_B T}{C \cdot OSR} \tag{3}$$

For a given SNR (dB), the minimum sampling capacitor size can be found [1]:

$$C_s = \frac{4k_B T \cdot 10^{SNR_{dB}/10}}{OSR \cdot (\mathrm{V}_{DD} \cdot \mathrm{OL})^2} \tag{4}$$

Where OL is overloading factor to ensure modulator stability and SNR defines as follow:

$$SNR = 10\log\left(\frac{(V_{DD} \cdot OL)^2 \cdot OSR \cdot C_S}{4k_B T}\right) \tag{5}$$

Switches are also an important source of no idealities in SC circuits, especially in low-power circuits. The switch gate area should be small to reduce charge injection and clock feed trough from the gate capacitor, while the on-resistance should be small enough to allow the capacitor voltages to settle within a small and constant error. As settling occurs quickly compared to the signal frequency due to oversampling, it is assumed that V_{IN} is a constant at the sampling time. The allowed error can be found in [1], and total time allowed for settling is:

$$t_s = \frac{\alpha}{f_s} \tag{6}$$

The allowed time constant τ_{total} for the worst case (OL· VDD) can then be found as:

$$\tau_{total} = \frac{t_s}{\ln\left(\frac{OL \cdot V_{DD}}{2V_e}\right)}$$
$$V_e = \frac{OL \cdot V_{DD}}{2 \cdot 10^{SDR_{dB}/20}} \tag{7}$$
$$SDR = 20\log\left(\frac{OL \cdot V_{DD}}{2V_e}\right)$$

So we can obtain maximum allowed switch resistance for the two sampling switches (Φ_1 phase):

$$R_{s1} + R_{s2} = \frac{\tau_{total}}{C_1} \tag{8}$$

To find the required coarse current we can assume that the output ramp is constant so we can write[2]:

$$V_{out} = \frac{I_{coarse}}{C_{out}} \cdot t$$
$$I_{coarse} = \frac{C_{out}\left(V_{pp}/4 + V_{cm}\right)}{\frac{1}{2f_s} - T_r} \quad (9)$$

Where T_r is the reset time, f_s is sampling frequency, V_{cm} is the common mode voltage, V_{pp} is the differential peak-to-peak signal swing and C_{out} is the output equivalent capacitor given by [2]

$$C_{out} = C_{Load} + \frac{C_1 C_2}{C_1 + C_2} \quad (10)$$

The comparator delay is chosen based on technology and noise properties [2]. The required output resistance of the current source is determined by the gain error from (8) and we can conclude (11).

$$R_o = \frac{-T_d}{\ln\left(1 - e_g\right) \cdot C_{out}}$$
$$1 - e_g = e^{-T_d / R_{out} C_{out}} \quad (11)$$

Finally the comparator offset and comparator threshold can be calculated as follows [2]

$$V_{off} = I_{coarse} R_{out} \left(1 - e^{\frac{-T_d}{R_{out} C_{out}}} \left(1 + 2\frac{V_{ct}}{I_{coarse} R_{out}}\right)\right)$$
$$V_{ct} = -1/2 I_{coarse} R_{out} \left(1 - e^{\frac{T_d}{R_{out} C_{out}}}\right) \quad (12)$$

4. Logic Part of CBSC Integrator

Logic part of CBSC integrator generates control signals. For design this part we should know about time sequence of signals. Generally comparator output and Φ_2 are inputs and P, E1, E2 and S are outputs of this part (fig.4). Figure 5 is the timeline of control signals:

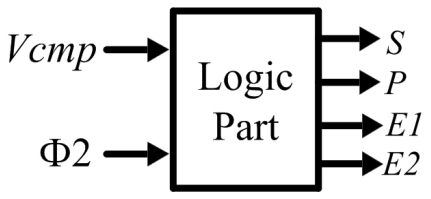

Fig.4 Logic part of CBSC integrator

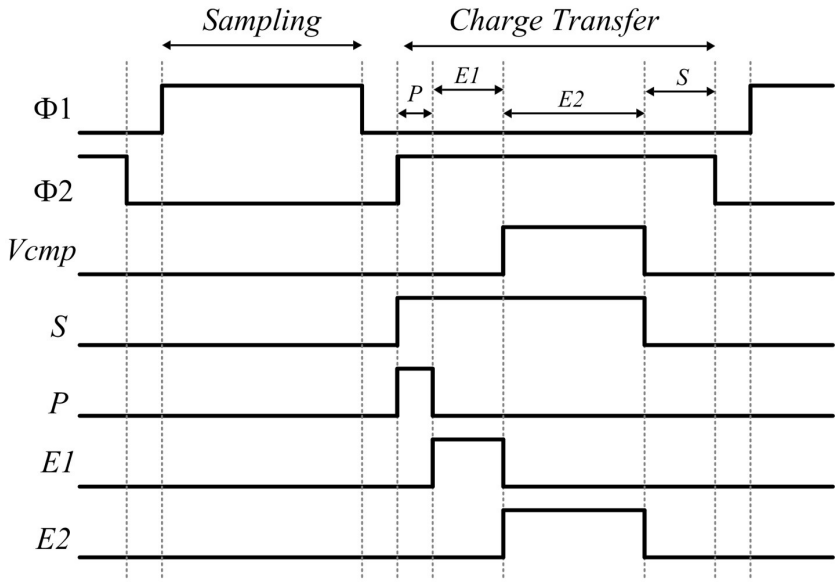

Fig.5. Timeline of CBSC Integrator Signals

For generating P the bellow logic circuit has been suggested.

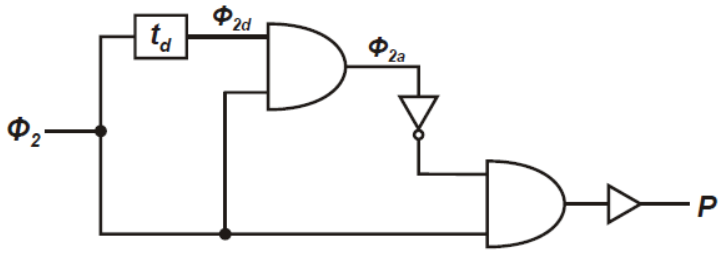

Fig.6. Logic circuit for making P

E2 and S can generate by using a NAND gate, AND gate and a D type flip-flop as follow:

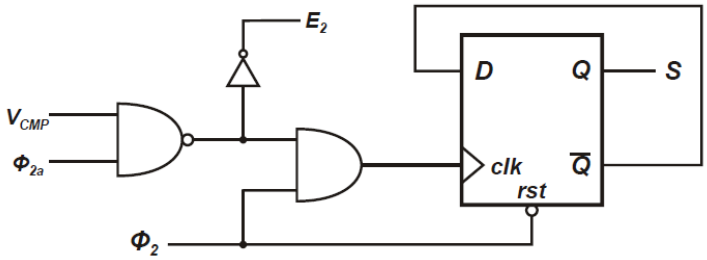

Fig.7. Logic circuit for making E2 and S

Finally E1 generate by one XOR gate and a AND gate like bellow:

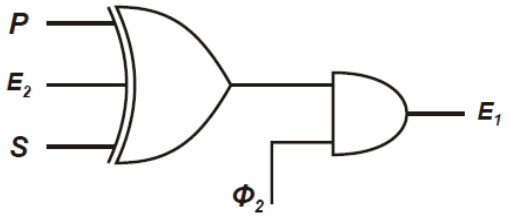

Fig.8. Logic circuit for making E1

5. A Design Example for CBSC Integrator

As an example we design a CBSC integrator by using above equations. With T=300K the calculated parameters are in table1.

Table1. SUMMARY OF CALCULATED PARAMETERS

Technology target	180nm CMOS
Supply voltage	1.8 V
Sampling frequency	5 MHz
I_{Coarse}	80 µA
I_{Fine}	10 µA
T_d	2 nS
R_{out}	1 MΩ
C_s	100 fF
C_2	400 fF
C_{Load}	1 pF
V_{ct}	41 mV
V_{cm}	0.64 V

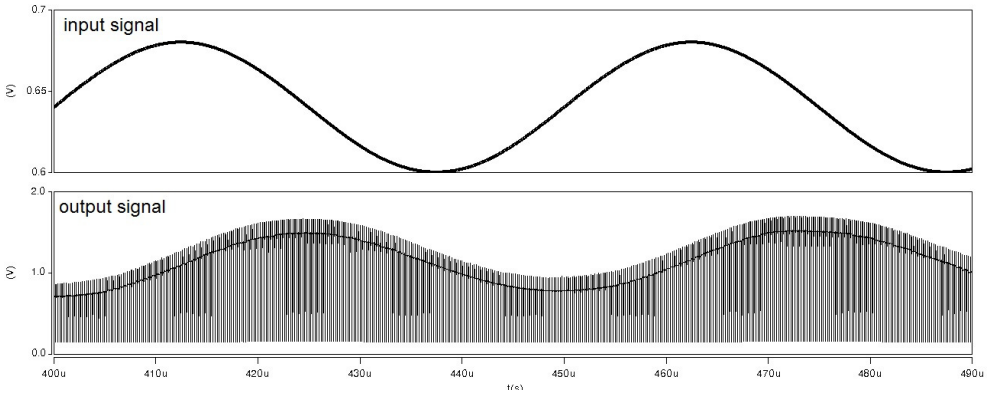

Fig.9. input and output of CBSC integrator in time domain.

6. Conclusions

Design equations for CBSCI are presented. In this paper we have shown how one can calculate the parameters for CBSC integrator for use in a Sigma-Delta ADC. The parameters are

capacitance (C), current (I), comparator delay (Td), current source output resistance (Ro) and comparator threshold (Vct). In addition the design equations have been verified with simulation by HSPICE and using 0.18μ CMOS technology

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