DELAY TIME ANALYSIS OF COMBINED CMOS RING OSCILLATOR

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ABSTRACT

CMOS ring voltage controlled oscillator with combined delay stages is presented. Initially the general condition of oscillators is discussed then two common inverters are introduced and their delay times are calculated parametrically. Our analysis and parametrically calculations states that delay time of basic type inverter changes in opposite direction compared with current starved inverter versus supply voltage changing, so a combined schematic can be used to obtain better frequency stability. The result of simulation by TSMC 0.18μm CMOS technology and HSPICE approve the analysis results. The simulated proposed CMOS VCO reduced the oscillation frequency dependence to supply voltage considerably and is appropriate for On-Chip applications since no passive element is used.

KEYWORDS

CMOS Ring Oscillator, Frequency Stability, CMOS Inverter, Delay Time

1.INTRODUCTION

Voltage control oscillator (VCO) is one of the most significant part of any digital and analog systems [4,5,6,7].While there are several structures for design of oscillators, one of the most common structures is the ring oscillators which can be used as clock in systems [4].

The most significant advantage of full transistor oscillator is the issue that this type of oscillator is compatible with integration and there is no passive element such as capacitor or inductor [12, 13, 14, 15, 16, 17, 18]. This feature is important due to the fact that die area in CMOS technology is a really important factor and full transistor circuits occupy less area in chip [1,4,5].
This paper initially discusses the general condition for oscillation then parametrically calculates the delay time of two common inverters. Then shows that a combined configuration for CMOS ring oscillator is more stable regarding oscillation frequency versus supply voltage variation. In fact the combined structure has less frequency deviation with noisy supply voltages. In addition simulation results verify the analysis findings.

A ring oscillator is made of some delay stages. An oscillator can be designed by odd number of single-input single-output delay stages or by even number of differential delay stages (Fig.1 & Fig.2).
Based on Barkhausen criteria every stage should add $180/N$ phase to the signal (or reduce) and the other $180°$ provided by the sign of inverters (N; number of stages are odd).You can have an oscillator with even numbers of delay stages by use of differential configuration with connections based on fig.2.

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We are able to design an oscillator with relatively high rejection of the common mode noise by using differential structure.

For calculating the oscillation frequency we can use (1) and (2).

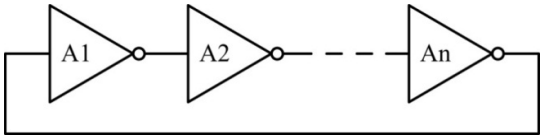

Fig 1. Ring oscillator by odd number of inverters [2]

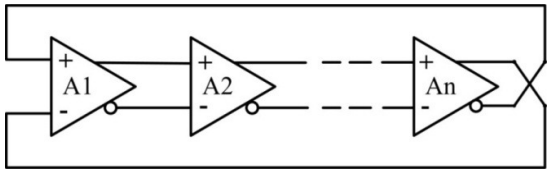

Fig 2 Ring oscillator by even number of stages [1]

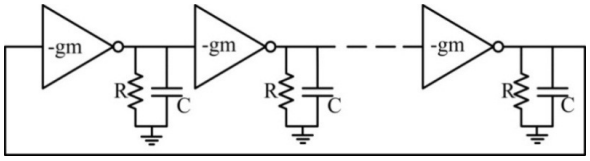

Fig 3. linear model of ring oscillator[1]

$$A_1(j\omega) = A_2(j\omega) = \ldots = A_N(j\omega) = \frac{-g_m R}{1 + j\omega RC} \quad (1)$$

$$\left|A_1(j\omega).A_2(j\omega).\ldots.A_N(j\omega)\right| = 1 \quad (2)$$

Also about the phase of oscillators we have:

$$\angle \mathrm{A1}(\mathrm{j}\omega) = \theta = \tan^{-1}(\omega \mathrm{RC}) = \frac{2K\pi}{RC} \quad (3)$$

$$\omega_0 = \frac{\tan\theta}{RC} \quad (4)$$

The above equations describe the start frequency of oscillation [2]. We need to calculate the stable oscillation frequency by using large signal analysis. So considering the delay time of stages becomes important. The oscillation frequency of an oscillator can be calculated as (5), which N is number of stages and t_d is delay time of stages.

$$f_0 = \frac{1}{2Nt_d} \quad (5)$$

It is obvious from (5) that oscillation frequency depends only stages delay time since the number of stage in a fixed structure is constant. So delay time is the most important parameter for studying full transistor ring oscillator.

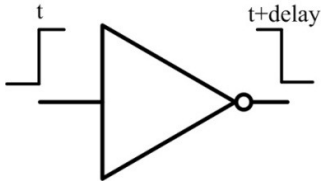

Fig 4. an inverter with delay time

2.DELAY TIMES

General conditions of oscillations were discussed in previous part. In order to design a ring oscillator according to structure in previous section, we have to use inverters as delay stages. Regarding the delay time as the most important parameter in this kind of oscillator we should better calculate the delay time of stages. With the assumption of two inverters, basic type and current starved inverters (Fig.6 and Fig.7), we have calculated the delay times for these inverters with the aim of Fig.5. This figure shows the ideal input and typical out puts for inverters. Let's assume that delay time is proportional to $t_2 - t_0$ so it's need to calculate $t_2 - t_0$ as delay time. So we have for basic inverter:

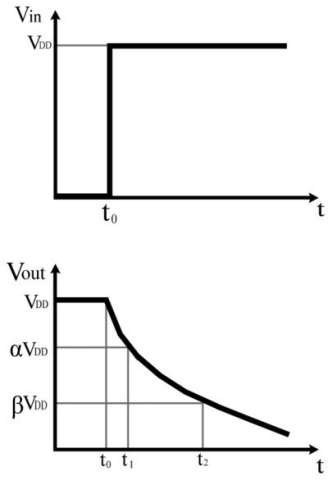

Fig 5 input pulse and output of inverter

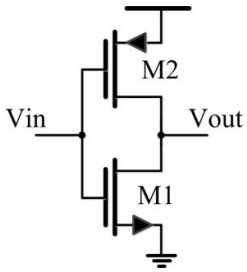

Fig 6 basic type inverter as a delay stage

C_L defines as total capacitance load connectes to output node, V_{th} represents threshold voltage of MOSFET,I_D states current of MOS transistors,C_{ox} represent total capacitance per unit length of MOSFET and μ defines mobility of charge carriers(electrons and holes).note that "n" subtitles belongs to NMOS and "p" subtitles belongs to PMOS transistor.

t0<t<t1 nmos →saturation

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})^2 = -I_{CL} = -C_L\frac{dV_{out}}{dt} \quad (6)$$

for $V_{DD}- V_{th}<V_{out}<V_{DD}$

$$\int_{t_0}^{t_1} dt = -C_L\int_{V_{DD}}^{\alpha V_{DD}}\frac{1}{I_{Dn}}dV_{out} \quad (7)$$

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{th})^2}\int_{V_{DD}}^{\alpha V_{DD}} dV_{out} \quad (8)$$

$$t_1 - t_0 = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{th})^2} \quad (9)$$

$t_1< t<t_2$ nmos →Linear

$$I_{Dn} = \mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})V_{out} = -\frac{1}{2}V_{out}^2 \quad (10)$$

$$\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})V_{out} - \frac{1}{2}V_{out}^2 = -C_L\frac{dV_{out}}{dt} \quad (11)$$

for $V_{out}<V_{DD}- V_{th}$

$$\int_{t_1}^{t_2} dt = -C_L\int_{\alpha V_{DD}}^{\beta V_{DD}}\frac{1}{I_{Dn}}dV_{out} \quad (12)$$

$$\int_{t_1}^{t_2} dt = -\frac{2C_L}{\mu_n C_{ox}\frac{W}{L}}\int_{\alpha V_{DD}}^{\beta V_{DD}}\frac{1}{2(V_{DD}-V_{th})V_{out}-V_{out}^2}dV_{out} \quad (13)$$

$$t_2 - t_1 = \frac{C_L}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \ln\left(\frac{2\alpha - \beta}{\beta}\right) \quad (14)$$

$$\alpha > \beta$$

$$(9) + (14) \Rightarrow delay\ time$$

$$t_{delay} \propto t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0)$$

$$t_{delay} \propto \frac{2C_L(1-\alpha)VDD}{\mu n\ Cox \frac{W}{L}(VDD - Vt)^2} + \frac{C_L}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \ln\left(\frac{2\alpha - \beta}{\beta}\right) \quad (15)$$

The same calculations are applied to current starved inverter.

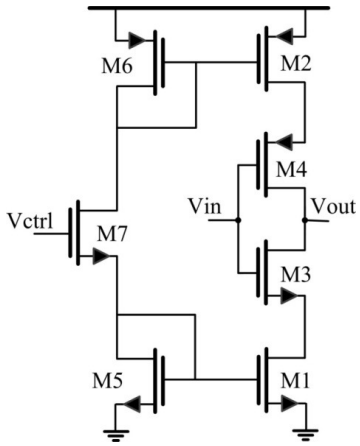

Fig 7 Current starved inverter as a delay stage [1]

We know that in current starved inverter, the gate voltage of M1 and M2 supplied through circuit bias and there is no dependency between this voltage and input or output. This voltage is determined by the current of M5 and M6, which V_{ctrl} controls this current.

$$t_0 < t < t_1 V_{in} = V_{DD}\ \&\ V_{out} = [V_{DD}, V_{DD} - V_t]$$

$$M3 \rightarrow saturation,$$

$$M1 \rightarrow saturation\ \ \&\ \ M4 \rightarrow cut\ off$$

Here, the current is determined by M1 but not M3.This is because current flow through M1 is determined by the current mirror formed by M1-M5 and is independent of the gate-source voltage of M3.

$$for V_{DD} - V_{th} < V_{out} < V_{DD}$$

$$V_{DD} - V_t = \alpha V_{DD} then\ 0 < \alpha < 1$$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs1} - V_{th})^2 \quad (16)$$

$$dt = -\frac{C_L}{\frac{1}{2}\mu_n C_{ox}\frac{w}{L}\left(V_{gs1}-V_{th}\right)^2}dV_{out} \tag{17}$$

$$\int_{t_0}^{t_1} dt = -C_L \int_{V_{DD}}^{\alpha V_{DD}} \frac{1}{I_{Dn}} dV_{out} \tag{18}$$

Know that $\left(V_{gs1}-V_{th}\right)$ is a constant value.

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{\mu_n C_{ox}\frac{w}{L}\left(V_{gs1}-V_{th}\right)^2}\int_{V_{DD}}^{\alpha V_{DD}} dV_{out} \tag{19}$$

$$t_1 - t_0 = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox}\frac{w}{L}\left(V_{gs1}-V_{th}\right)^2} \tag{20}$$

$t_1 < t < t_2$

$M3 \rightarrow linear \ \ \& \ \ M1 \rightarrow saturation$

$$I_{D3} = \mu_n C_{ox}\frac{w}{L}\left(V_{gs3}-V_{th}\right)V_{ds3} - \frac{1}{2}V_{ds3}^2 \tag{21}$$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}\left(V_{gs1}-V_{th}\right)^2 \tag{22}$$

$$I_{C_L} \cong -I_{D3} = C_L\frac{dV_{out}}{dt} \tag{23}$$

$for V_{out} < V_{DD} - V_{th}$

$$\int_{t_1}^{t_2} dt = -C_L \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{I_{D3}} dV_{out} \tag{24}$$

$$\int_{t_1}^{t_2} dt =$$

$$= -\frac{C_L}{\mu_n C_{ox}\frac{w}{L}}\int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{dV_{out}}{\left(V_{gs3}-V_{th}\right)V_{ds3} - \frac{1}{2}V_{ds3}^2} \tag{25}$$

$V_{ds3} = V_{out} - V_{ds1} \cong V_{out} and V_{gs3} \cong V_{in} = V_{DD}$

$$\int_{t_1}^{t_2} dt =$$

$$= -\frac{C_L}{\mu_n C_{ox}\frac{w}{L}}\int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{(V_{DD}-V_{th})V_{out} - V_{out}^2} dV_{out} \tag{26}$$

$$t_2 - t_1 = \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \frac{1}{(V_{DD} - V_{th})} \ln\left(\frac{\alpha - \beta}{\beta}\right) \quad (27)$$

$$(20) + (27) \Rightarrow delay\ time$$

$$t_{delay} \propto t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0)$$

$$t_{delay} =$$

$$\frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox} \frac{w}{L}(V_{gs1} - V_{th})^2} + \frac{C_L}{\mu_n C_{ox} \frac{w}{L}(V_{DD} - V_{th})} \ln\left(\frac{\alpha - \beta}{\beta}\right) \quad (28)$$

By assuming supply voltage deviation we can write:

$$\Delta t \quad of \quad Basic\ Inverter \cong \frac{A}{\Delta V_{DD}} + \frac{B}{\Delta V_{DD}} \quad (29)$$

$$A \cong \frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}}$$

& (30)

$$B \cong \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \ln\left(\frac{\alpha - \beta}{\beta}\right)$$

$$\Delta t\ of\ Current\ Starved\ Inverter \cong$$

$$D \times \Delta V_{DD} + \frac{B}{\Delta V_{DD}} \quad (31)$$

$$D \cong \frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}(V_{gs1} - V_{th})^2} \quad (32)$$

$$0 < (V_{gs1} - V_{th}) < 1 \rightarrow (V_{gs1} - V_{th})^2 \square\ 1$$

$$\frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}(V_{gs1} - V_{th})^2} > \frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}} \quad (33)$$

$$\frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}(V_{gs1} - V_{th})^2} > \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \ln\left(\frac{\alpha - \beta}{\beta}\right) \quad (34)$$

$$\ln\left(\frac{\alpha - \beta}{\beta}\right) < 1 \qquad then \qquad D > A \ \&\ D > B \quad (35)$$

As a final result,Δt of basic inverter is proportional with 1 / ΔV_{DD}, and Δt of current starved inverter is proportional with ΔV_{DD}. Regarding the delay times opposite variation for two mentioned inverters we can conclude that combined structure for ring oscillator is an appropriate technique to design a CMOS ring oscillator with decreasing the frequency deviation versus supply changing. As the fig.8 and fig.9 shows, the results are approved by the simulations. Fig.8

and fig.9 shows frequency deviation of VCO built with only one type inverter(basic and current starved) versus supply voltage (fig.8) and temperature(fig.9).

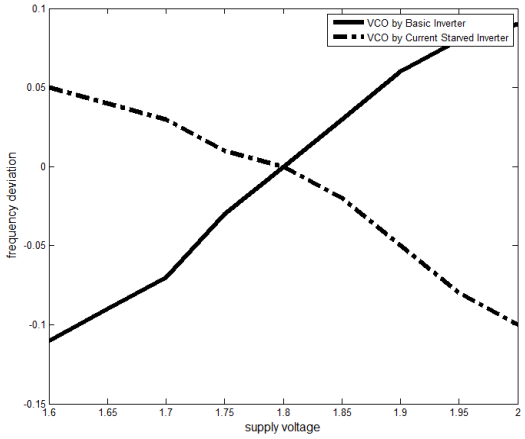

Fig 8 frequency deviation versus supply voltage

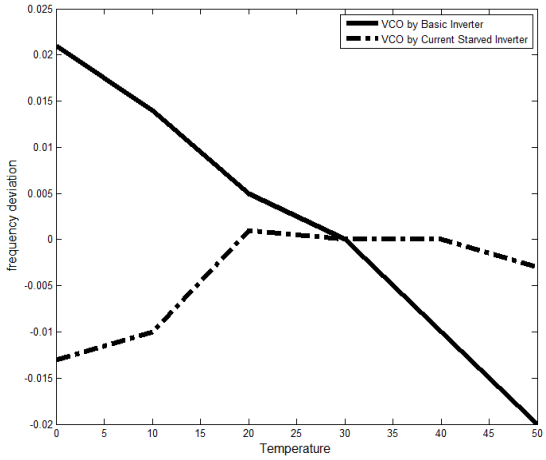

Fig 9 frequency deviation versus temperature

3.OSCILLATION FREQUENCY DEVIATION

Oscillation frequency of the CMOS ring oscillator based on delay time is described by (5), $f = 1/2NT_d$. So any deviation in the delay time leads to oscillation frequency deviation. In fact, this delay is sum of time delays of all inverters which made ring oscillator.

$$t_{delay} = t_{d1} + t_{d2} + t_{d3} + \ldots + t_{dn} = n \times t_d n = odd \quad (36)$$

Then, if all inverters are same type $t_1 \quad \cdots \quad t_2$ have same changing. It means all become smaller or bigger. As example, for three stages ring oscillator can be written:

$$t'_{delay} = t_{d1} + t'_{d2} + t_{d3} \quad (37)$$

Here the first and third time delay belongs to the basic inverter and are equal. Current starved inverter is owned t'_{d2}.The total time delay is the sum of these three times. Note that any change in

the supply voltage changes delay times but as these changes are added together, they can reduce the effects of one another. Namely for three stages we have:

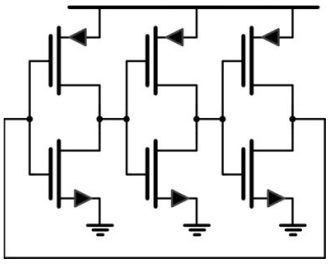

Fig 10.CMOS ring oscillator by three basic inverter($\Delta t_{delay} = 3\Delta t$) [11]

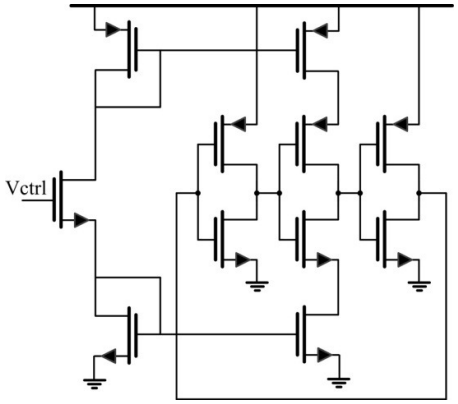

Fig 11 CMOS ring oscillator by two basic inverter and one current starved inverter ($\Delta t'_{delay} = 2\Delta t + \Delta t'$) [11]

Considering the (38), by using combined configuration we can reduce the frequency deviation versus supply voltage changing. In fact the combined structure has more accurate oscillation frequency.

$$\Delta t \uparrow \leftrightarrow \Delta t' \downarrow$$
$$\&$$
$$\Delta t \downarrow \leftrightarrow \Delta t' \uparrow \rightarrow \Delta T'_{delay} \cong cte \qquad (38)$$
$$f'_{osc} = \frac{1}{6t'_{delay}} \rightarrow f'_{osc} \cong cte$$

Frequency variations versus supply voltage for combined and basic ring oscillator have been shown in Fig.12. According to this figure combined configuration obtained better performance considering less frequency deviation. This can be verify by defining a factor as frequency deviation factor. Smaller value for this factor means better performance. It is obvious that combined ring oscillator has smaller value for this factor.

$$\frac{\Delta f}{f} = \frac{f\left(V_{DD} + \Delta V_{DD}\right) - f\left(V_{DD}\right)}{f\left(V_{DD}\right)} \qquad (39)$$

$f(V_{DD}+\Delta V_{DD})$ is oscillation frequency when supply voltage is $V_{DD}+\Delta V_{DD}$.

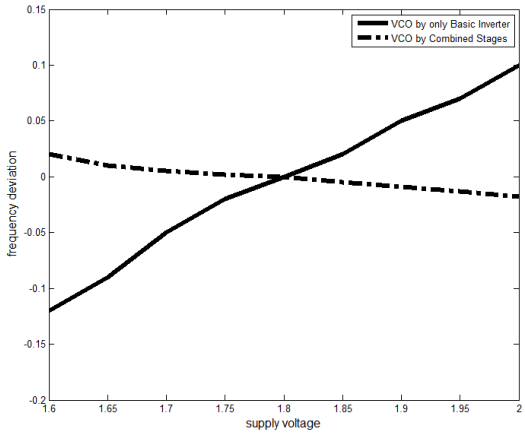

Fig 12 frequency deviation versus supply voltage for fig.10 & fig.11 oscillators

4.CONCLUSION

Ring oscillators are the basic blocks of integrated circuits. Delay calculations for two common CMOS inverters as delay stages have been presented in this paper. Then by considering the delay analysis a combined structure for CMOS ring oscillator has been proposed. The proposed combined configuration shows a better performance regarding the frequency deviation versus supply voltage changing. Also the analyses have been verified by simulation results. The presented combined ring oscillator has been simulated with HSPICE and 180nm CMOS technology. The simulation results in tab.1 presents comparing between the simple types oscillator and combined oscillator.

Table 1 Comparison of simple types and combined ring oscillators

Number of stages	3	3
Basic type inverter	3	2
Current starved inverter	0	1
Number of transistor	6	11
$\frac{\Delta f}{f}$ (V_{DD})	8%	2%
$\frac{\Delta f}{f}$ $(TEMP)$	3%	0.5%

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