

ANALYTICAL DISTINCTION BETWEEN CNTFET BASED AND MOSFET BASED SRAMS AND LOGIC GATES

Turja Nandy*, Arin Dutta, Zahid Hasan Mahmood

Electrical and Electronic Engineering, University of Dhaka
Dhaka 1000, Bangladesh

ABSTRACT

In this review, we compare the distinct properties of Carbon Nanotube Field Effect Transistor (CNTFET) based applications with MOSFET based applications in memory and digital electronics technology. In nanoelectronics circuitry, CNTFET has opened new dimensions with extreme opportunities of improvement in circuit performance due to its extreme mobility, ballistic conduction and so forth. Apart from being an excellent conductor, CNTFET can also be used as a memory unit for its good stability in storing a data bit and as digital circuits (multi-valued logic gates) for its better PDP and sensitivity. This paper discusses the design and read-write mechanisms of 6T and 8T CNTFET SRAM cell and a comparative study among themselves based on their corresponding advantages and disadvantages. Moreover, superiority of CNTFET SRAM over MOSFET SRAM is analyzed in terms of certain phenomena (such as scattering, defect-tolerance and ability to work in low power supply) observed in them. At last, different types of ternary logic gates and how they will persevere the limitations of MOSFET logic gates with its PDP value, less power dissipation and better longevity have been discussed.

KEYWORDS

CNTFET, SRAM, SNM, ternary logic, PDP.

1. INTRODUCTION

Since the invention and fabrication of Carbon Nanotubes (CNT) in 1991 by Japanese researcher Sumio Iijima and later on by Al Harrington and Tom Maganas, it has been an attractive topic of research for researchers and engineers across the world. Following that, it has constantly been experimented to be used in nanoelectronic devices to overcome the limitations of conventional silicon devices. In recent years, CNTFET has also been introduced in memory technology and digital electronics. SRAM and logic gates are such applications which can be structured by CNTFET. Because of its ability to store data for longer period and less power delay product, CNTFET has emerged as a possible and promising replacement of MOSFET in structuring memory devices including storage cells [1]. Memory cells like SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory) have been designed in different ways with different architectures (actually different number of transistors) along the years. Again, to perform digital operations, logic gate is an inevitable part in design procedure and CNTFET can also be implemented in multi-valued logic gate architecture for its tremendous performance over

MOSFET based logic gates [2]. This provides a considerable amount of overall performance improvement in digital logic circuitry [3].

2. TRADITIONAL SRAM (6T SRAM) CELL DESIGNED BY CNTFET

One of the best applications of CNTFET is using it to construct memory storage devices such as SRAM. In nanoscale fabrication, to overcome the poor performances and limitations encountered while dealing with MOS technology, SRAM designed by CNTFET has been proposed [4],[5].

2.1. Design

A traditional 6T (six transistors) CNTFET SRAM cell is a memory cell which can be used in most register file and cache designing. In Fig. 1, the design of a traditional CNTFET SRAM is given. Here, six CNTFETs are structured such a way where four of them form an individual SRAM cell (basic memory cell) architected as two cross coupled inverters and the other two CNTFETs are used to operate the read and write functions of the memory cell. Read and write mechanisms of SRAM designed by CNTFET is identical to traditional MOSFET SRAM [4],[5].

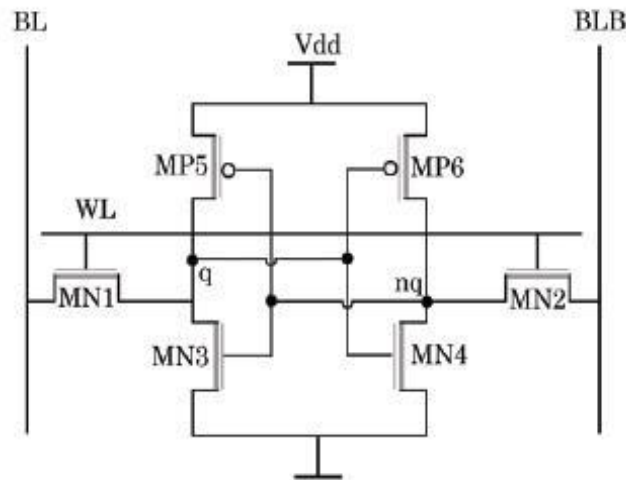


Fig 1.6T SRAM cell designed by CNTFET [5]

2.2. Read operation

Initially, BL and BLB bit lines are pre-charged to logic 1. Then, word line WL is made high. So access transistors MN_1 & MN_2 become active and data (whatever 1 or 0) stored at the SRAM is read. In read operation, data bit stored at SRAM cell can be changed due to read upset problem. For example, considering that the cell has stored 1, i.e. node nq is 1 and q is 0. When WL is 1, then both MN_1 and MN_2 become high and the node q will become high which was previously low. To remove this problem, proper sizing ratio has to be maintained between MN_3 and MP_5 such that the voltage level at the node q may not be altered [4],[5].

2.3. Write operation

To write data bit in SRAM cell, the word line WL is kept high which allows storing data (0 or 1) from bit line BL and BLB to the SRAM cell. The pull up transistor (MP_6) shouldn't be much strong than the access transistor (MN_2) to write data in SRAM. For example: consider SRAM is storing 0 and 1 has to be written in the SRAM cell. So the node nq is to be gone to low state (0). As a result, it is clear that the MN_2 transistor has to be much conductive than MP_6 . To write data properly in SRAM cell without altering any bits, proper sizing ratio has to be kept between MN_2/MP_6 [4],[5].

3. 8T SRAM CELL DESIGNED BY CNTFET

For performing faster operation, extra transistors are added with traditional CNTFET SRAM. Fig. 2 shows 8T CNTFET SRAM which is one of them. In 8T CNTFET SRAM, read and write ports are separated by RWL and WWL word lines respectively. These lines are used to access data bits for read and write operations [6],[7].

3.1. Read operation

Prior to the read operation, the read bit line (RBL) is made high (logically 1). Read operation is started by asserting the RWL line. The RBL may remain in HIGH state or become LOW state depending on the data which is read from the basic memory cell or the internal node of the basic SRAM cell [6],[7].

3.2. Write operation

Before the write operation, the write bit lines (WBL) are pre-charged to the values (0 or 1), which are to be written in the cell. By asserting the write word line (WWL), write operation starts. Then the basic SRAM cell or internal nodes of the memory cell get their corresponding values from WBL lines and write operation is performed [7].

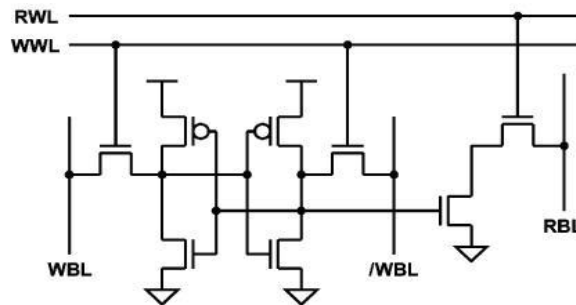


Fig 2.8T SRAM cell designed by CNTFET [8]

4. ADVANTAGES AND DISADVANTAGES OF 8T CNTFET SRAM OVER 6T CNTFET SRAM

8T SRAM by CNTFET has been designed for the fact that, it is more immune to noise voltage during read operation and ensures non-destructive read operation than traditional 6T SRAM cells. 8T SRAM also provides effective memory speed . Fig. 3 shows that static noise margin is worst in the read operation of 6T CNTFET SRAM. In 8T CNTFET SRAM, better static noise margin can be possible than 6T SRAM [8],[9].

Extra transistors are added for improving the performance of a traditional CNTFET SRAM. But, there are also some disadvantages happened along with it. In 8T SRAM cell, large number of transistors is used. So the area of the SRAM cells increase and large power is dissipated by these memory cells. Moreover, working principles of them are more complex than 6T CNTFET SRAM cells [9] [10].

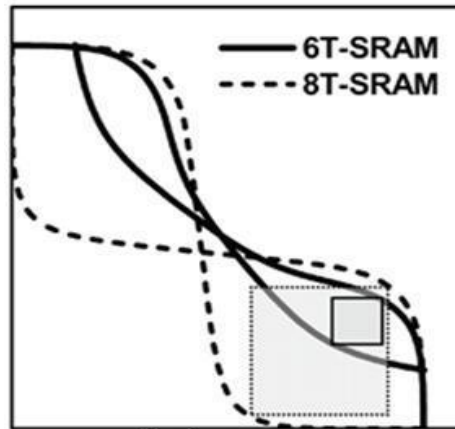


Fig 3.SNMs of 6T and 8T CNTFET SRAM [8]

5. COMPARISON BETWEEN CNTFET SRAM AND MOSFET SRAM

In Nanotechnology, due to scaling down devices into nano range, various problems have been occurred dealing with traditional 6T SRAM of CMOS technology for its read/write instability, less speed, low power supply problem etc. To overcome these problems of MOSFET, CNTFET SRAM can be a good replacement of MOSFET SRAM [4],[7],[11].

5.1. Defect-tolerance

Without changing the stored bit, CNTFET SRAM cell can tolerate the maximum dc noise voltage. This defect-tolerance is occurred by controlling the threshold voltage as well as controlling chiral vector and chiral angle. This type of SRAM is called Dual-Chirality SRAM cell (PCNTFET & NCNTFET) [5]. By varying diameter of CNTs, PCNTFET & NCNTFET can be obtained. When defective voltage is generated, then flipping from PCNTFET to NCNTFET or vice-versa takes place for suppressing the defect. Apart from dual-chirality SRAM cells, now-a-

days, another configuration is structured to achieve the defect tolerance which is called Quadded-transistor structure. Here, to tolerate the defects (stuck-open/short, AND/OR bridge), quadded structure replenishes each transistor. On the contrary, MOSFET cannot exhibit defect-tolerant property due to its structural limitations [5].

5.2. Less scattering

Channel length of CNTFET is very small compared to the MFP (mean free path) of intrinsic CNT for elastic scattering, acoustic scattering and optical photon scattering. So carriers face less scattering while flowing through the intrinsic CNT, which provides ballistic transport of carriers. As a result, when SRAM is manufactured from CNTFET, it provides large speed due to less scattering of charge carriers [11]. Due to absence of ballistic transport phenomena, when temperature increases, the carriers propagating through the channel face scattering. This scattering increases proportionally with temperature and hence peak carrier mobility decreases resulting low on-current density which is found in CMOS devices and this causes a low speed for SRAM based on MOSFET [11].

5.3. Low power supply

In nano scale fabrication, very low power supply is sufficient to manufacture nano devices in memory technology. This is a huge problem for traditional SRAM because MOSFET SRAM can't work better in low power supply. In this case, CNTFET SRAM is a better choice [4].

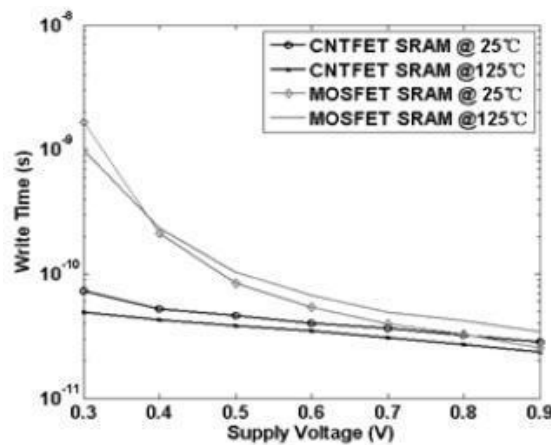


Fig 4.(a) Write time vs supply voltage curves for CNTFET based and MOSFET based SRAM for different temperatures [4]

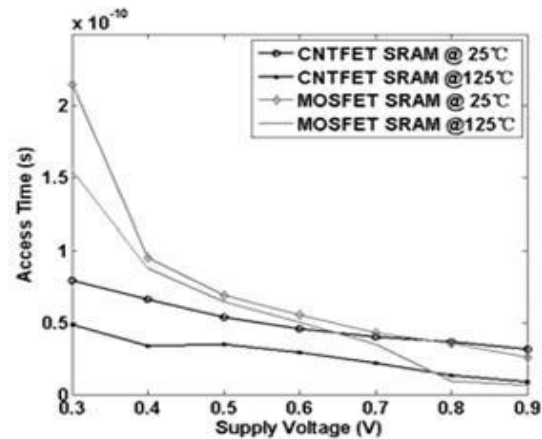


Fig 4.(b) Access time vs supply voltage curves for CNTFET based and MOSFET based SRAM for different temperatures [4]

Fig. 4(a) & 4(b) shows this comparative study. Here, due to low electric field, the write time of MOSFET SRAMs increases quickly at low power supply (at 0.3V). But this time decreases according to the increase of supply voltage and at high supply, both write times are almost same (0.9V). So when voltage of power supply is low, write and access delay is found in MOSFET SRAM [4].

5.4. Better stability

CNTFET based SRAM has shown very tremendous stability compared to the MOSFET based traditional SRAM [5]. When a data bit is read from/write in a SRAM cell, data retention is very important for stable access. As in low power supply application, MOSFET SRAM becomes less stable, so it can't be operated properly. But CNTFET SRAM can show better and stable read operation in case of low power supply. If the SRAM cell can hold data bit against noise, the device is said to be stable, which is measured in terms of static noise margin (SNM). Minimum noise that is present in the internal nodes of basic SRAM cell to alter the state of the cell is defined as SNM [7].

Fig. 5 shows the SNMs of MOSFET SRAM. If dc noise voltage is present in two internal nodes of two cross coupled inverters of 6T SRAM cell, then Fig. 5 shows that the voltage transfer characteristics (VTC) of one inverter (right inverter, green curve) superimposes on the inverse VTC of another inverter (left inverter, blue curve). This curve is called "Butterfly Curve". But in CNTFET SRAMs, the area of two wings of this curve is larger than MOSFET SRAMs and that's why SNM is maximized and they withstand larger noise voltage. Consequently Read/Write function is very much stable in CNTFET based SRAM and can hold data for long time [7]

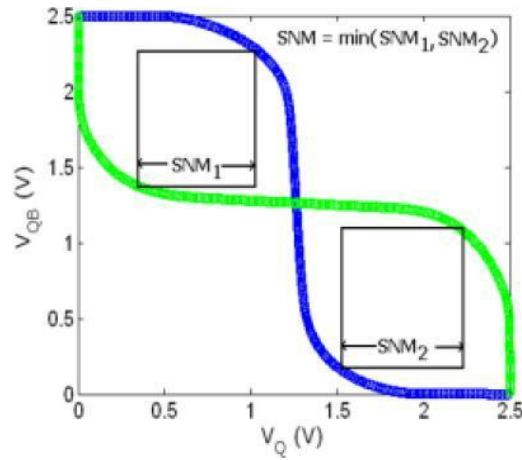


Fig 5.Static Noise Margin of MOSFET SRAM [7]

5.5. Flexibility of structure

CNTFET structure requires significantly less area than MOSFET. In case of CNTFET, there are better chances to control its structure by changing its chiral vector as well as the diameter of CNT which is absent in MOSFET. Large diameter can offer us an advantage of less read delay which gives a highly better performance in read operation for CNTFET SRAM than MOSFET SRAM. Fig. 6 shows the dependency of read delay on the diameter of CNT. Here it can be seen that by varying the diameter to greater values, read delay can be reduced [12].

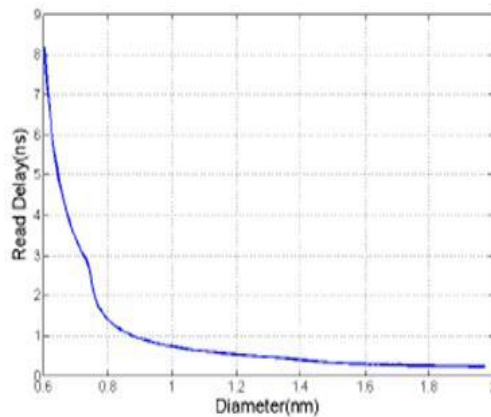


Fig 6.Response of read delay time according to the different diameters of Carbon Nanotube [12]

$$O_{NOR} = \overline{\max\{i_1, i_2\}} \quad (1)$$

6. LOGIC GATES BASED ON CNTFET

Although binary logic (0 or 1, true or false) is generally used to design digital systems, but now multi-valued logic becomes a better choice which is easily obtained by CNT. For example, ternary logic (three valued logic) has become more attractive for digital computation. Ternary logic is also known as fuzzy logic. Ternary logic is more efficient than binary logic in case of digital circuit simplicity, faster serial/parallel arithmetic operations, energy efficiency, reduction of power dissipation etc. By introducing a third value in binary logic, ternary logic can be obtained. Here, the ternary logic is represented by: 0, 1, 2 where 0 means FALSE, 1 means Undefined and 2 means TRUE. In terms of voltage levels, 0 = ground potential, 1 = 2.5 V, 2 = 5 V [13],[14]. In a CNTFET, multi threshold voltage can be obtained by varying the chiral vector as well as diameter of the CNT. Using these multi threshold CNTFETs, ternary logic gates can be implemented. In a resistible load CNTFET based ternary logic gate, very large value of external resistance is needed to satisfy the current requirement of CNTFETs. Basic arithmetic and logic operations such as: Arithmetic addition and subtraction, AND, OR, NOT, NAND, NOR etc. can be performed in ternary logic [13],[14].

6.1. Ternary NOR gate

NOR gate is a logic circuitry used in digital electronics applications. Ternary NOR gate is three valued NOR gate which is an improved version of binary NOR gate. The outputs of a ternary NOR gate can be determined using this equation [15],[16]:

$$O_{NOR} = \overline{\max\{i_1, i_2\}} \quad (1)$$

6.2. Ternary NAND gate

NAND gate is a universal gate. Ternary NAND gate is a better version which can be operated by three types of input. The function of two entry ternary NAND gate is defined by the following equation [15],[16]:

$$O_{NAND} = \overline{\min\{i_1, i_2\}} \quad (2)$$

6.3. Ternary NOT gate/inverter

Ternary inverter is one of the spectacular examples of Carbon Nanotube Field Effect Transistor based logic gates. The output of this ternary inverter is defined by a equation. In a ternary inverter, if i is the input and three outputs are a , b and c , then they can be obtained from these three equations [16],[17] which are given below:

$$a = C_2(i) = \begin{cases} 0, & \text{if } i = 0 \\ 2, & \text{if } i \neq 0 \end{cases} \quad (3)$$

$$b = C_0(i) = \begin{cases} 2, & \text{if } i = 0 \\ 0, & \text{if } i \neq 0 \end{cases} \quad (4)$$

$$c = C_1(i) = \bar{i} = 2 - i \quad (5)$$

TABLE 1. Ternary NOR and NAND outputs.

Input (i_1)	Input (i_2)	ONOR	ONAND
0	0	2	2
1	0	1	2
2	0	0	2
0	1	1	2
1	1	1	1
2	1	0	1
0	2	0	2
1	2	0	1
2	2	0	0

TABLE 2. Different ternary inverter outputs.

Input (i_1)	Output of PTI (a)	Output of NTI (b)	Output of STI (c)
0	2	2	2
1	2	0	1
2	0	0	0

Here, three outputs tell us about three types of inverter which are needed to implement the ternary inverter. The inverter for 1st output (a) is called Positive Ternary Inverter (PTI), second one (b) is called Negative Ternary Inverter (NTI) and the last one (c) is called Standard Ternary Inverter

(STI) [13]. The outputs of ternary NOR, NAND and NOT gates are shown in a truth table given in TABLE 1 and TABLE 2 [14],[16],[17].

7. CNTFET LOGIC GATES VERSUS MOSFET LOGIC GATES

In digital electronics applications such as logic gates, MOSFET is a highly used element. But in nanotechnology, MOSFET based logic gates face some problems as like as others. That is why it will need to be replaced and for this, the CNTFET based logic gates have been introduced. CNTFET based logic gates have some extraordinary merits over MOSFET based logic gates [3],[13],[14].

7.1. Power delay product (PDP) and Sensitivity

Due to complexity in the circuitry of logic gates, power consumption and power delay product (PDP) of the logic gates are necessary factors to consider. In case of MOSFETs and CNTFETs of same channel length, PDP of MOSFET based logic gates is 90-100 times greater than the PDP of CNTFET based logic gates [13].

Fig. 7(a) and Fig. 7(b) shows PDP Vs supply voltage curve of CNTFET logic gates and MOSFET logic gates respectively. Here PDP of CNTFET logic gates decreases at low power supply whether for MOSFET logic gates it increases. That is why, in nanofabrication, low power consumption for CNTFET logic gate is occurred which is a great advantage over fabrication of logic gates based on CMOS technology [13]. As the power delay product (PDP) of CNTFET based inverter and other logic gates is less than the PDP of MOSFET based logic gates, so the sensitivity of CNTFET logic gates to the supply voltage is slightly greater than MOSFET logic gates because sensitivity of a logic gate is such property which depends in the value of PDP [3],[13].

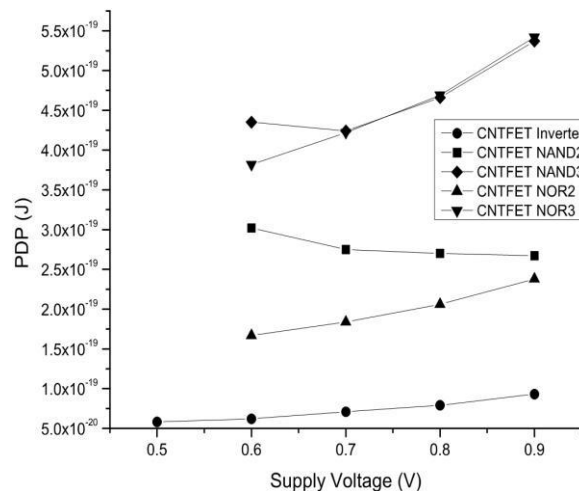


Fig 7.(a) PDP vs supply voltage curves of CNTFET based logic gates (NOR, NAND, NOT) [13]

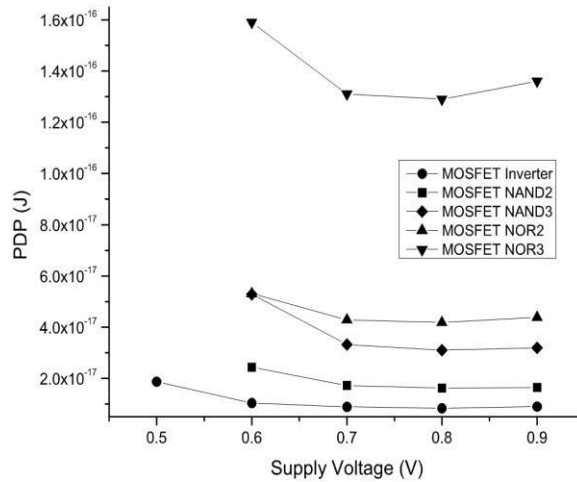


Fig 7.(b) PDP vs supply voltage curves of MOSFET based logic gates (NOR, NAND, NOT) [13]

7.2. Probability of destroying

The power delay product as well as power dissipation of MOSFET based logic gates increases with rising the temperature, though in case of CNTFET based logic gates, power delay product (PDP) and power dissipation remains constant with increasing temperature [13].

Fig. 8(a) and Fig. 8(b) shows this remarkable performance of CNTFET based logic gates against MOSFET based logic gates. The higher the temperature, the greater is the power consumption as well as heat dissipation for MOSFET based logic gates. Greater heat dissipation causes greater possibility of destroying the device. That is why the probability of destroying of MOSFET based logic gates at high temperature is larger than CNTFET based logic gates [13].

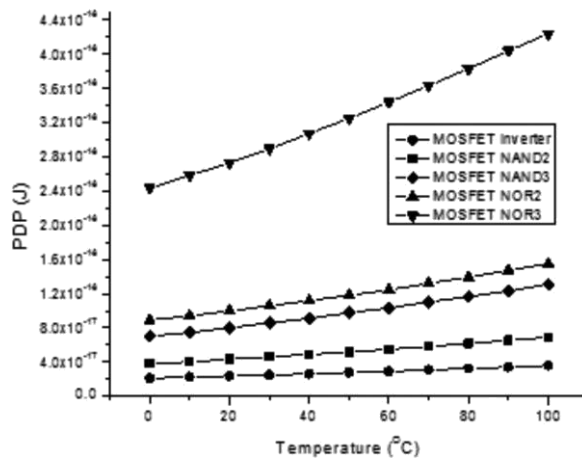


Fig 8.(a) PDP vs temperature curves of MOSFET based logic gates (NOR, NAND, NOT) [13]

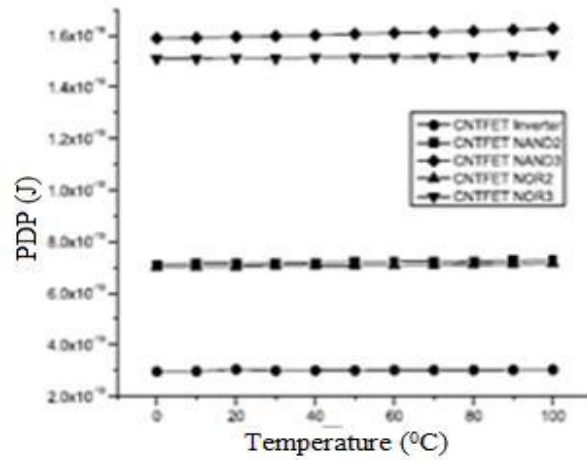


Fig 8.(b) PDP vs temperature curves of CNTFET based logic gates (NOR, NAND, NOT) [13]

7.3. Leakage power and Voltage gain

In case of power dissipation, leakage power is an important aspect to consider. Maximum leakage power of MOSFET based logic gates is much greater (about 70-80 times) than CNTFET based logic gates. So, power dissipation in MOSFET logic gates is higher than that of CNTFET logic gates. On the other hand, voltage gain of inverter (NOT gate) under CNTFET configuration is greater than MOSFET based inverter (NOT gate) which is happened nearly 3dB observed from their frequency response [3],[13].

8. CONCLUSION

In this study, we deliver the basic design and functionalities of two types of CNTFET SRAMs (6T and 8T). The paper has also reviewed the comparative properties of CNTFET SRAM and its superiority over MOSFET. From the discussion it is evident that despite less density, 8T SRAM cell provides better performance over 6T cell because of greater speed and noise immunity. Above all, it would be concluded that CNTFET SRAM comes up with extremely high efficiency compared to MOSFET SRAM because of its defect-tolerance, less scattering advantage and no low supply problem. Moreover, implementation of ternary logic gates with CNTFET is much more efficient with its better PDP, sensitivity and less probability of destroying than traditional Si MOSFET based logic gates technology. These performances may be considered as remarkable and promising factors for memory and digital applications in electronic devices in nanoscale range.

REFERENCES

- [1] S. L. Murotiya, A. Matta and A. Gupta, "Performance Evaluation of CNTFET-Based SRAM Cell design", Int. Conf. on Elec. Engg. and Comp. Sci. (ICEECS-2012), ISBN No. 978-93-81693-58-2, May 2012.

- [2] Y. B. Kim, "Integrated Circuit Design Based on Carbon Nanotube Field Effect Transistor", Transactions on Electrical and Electronic Materials, Vol. 12, No. 5, pp. 175-188, October 25, 2011, pISSN: 1229-7607, eISSN: 2092-7592.
- [3] S. K. Sinha and S. Choudhury, "CNTFET based Logic Circuits: A Brief Review", Int. Jour. of Emerging Tech. and Adv. Engg. (IJETA), ISSN 2250-2459, Volume 2, Issue 4, April 2012.
- [4] S. Lin, Y. B. Kim and F. Lombardi, "A New SRAM Cell Design Using CNTFETs", ISOC, IEEE, 2008, 181-182.
- [5] Suba R. B. and Sumam M. J., "Defect-tolerant SRAM Cell using CNTFETs".
- [6] N. S. Bhat, "Design and Modelling of Different SRAMs based on CNTFET 32nm technology", International Journal of VLSI design & Communication Systems (VLSICS), Vol.3, No.1, February 2012. 1971.
- [7] A. Gadhe and U. Shirode, "Read stability and Write ability analysis of different SRAM cell structures", Int. Jour. of Engg. Res. and Apps. (IJERA), ISSN: 2248-9622, Vol. 3, Issue 1, January-February 2013, pp.1073-1078.
- [8] K. Zhang, K. Chen, W. Pan and P. Ma, "A research of Dual-Port SRAM cell using 8T".
- [9] D. Aggarwal, P. kaushik and N. Gujran, "A Comparative Study of 6T, 8T and 9T Sram Cell", Int. Jour. of Latest Trends in Engg. and Tech. (IJLTET), ISSN: 2278-621X, Vol. 1, Issue 2, July 2012.
- [10] S. Lin, Y. B. Kim and F. Lombardi, "A Low Leakage 9T SRAM Cell for Ultra-Low Power Operation".
- [11] A. Pushkama, S. Raghavan and H. Mahmoodi, "Comparison of performance parameters of SRAM designs in 16nm CMOS and CNTFET technologies", IEEE, 2010.
- [12] H. Shahidipour, Y. Zhong, A. Ahmadi, K. Maharatna, "Effects of CNT Diameter Variability on a CNFET Based SRAM", Asia Pac. Conf. on Cir. and Sys. (APCCAS 2010).
- [13] Y. B. Kim, "Integrated Circuit Design Based on Carbon Nanotube Field Effect Transistor", Transactions on Electrical and Electronic Materials, Vol. 12, No. 5, pp. 175-188, October 25, 2011, pISSN: 1229-7607, eISSN: 2092-7592.
- [14] S. Lin, Y. B. Kim and F. Lombradi, "CNTFET-based Design of Ternary Logic Gates and Arithmetic Circuits".
- [15] A. Heung and H. T. Mouftah, IEEE J Solid-State Circuits, SC-20, 609 (1984).
- [16] S. Lin, Y. B. Kim and F. Lombardi, "A Novel CNTFET-Based Ternary Logic Gate Design".
- [17] P. C. Balla and A. Antoniou, IEEE J Solid-State Circuits SC-19,739 (1984).