

MULTIFUNCTION FILTER DESIGN USING BDQFG MILLER OTA

Nikhil Raj and Anil Kumar Gupta

Department of Electronics and Communication Engineering, NIT Kurukshetra,
Kurukshetra, India

ABSTRACT

In this paper, a low power bulk-driven quasi-floating gate MOSFET based Miller compensated Operational Transconductance Amplifier (OTA) is proposed required particularly in design of Gm-C filter. The analysis of amplifier is compared with low power bulk-driven technique. The performance comparison indicates that bulk-driven quasi floating gate configuration offers better performance. In this configuration the combination of bulk-driven input with quasi-floating gate results in improved transconductance and hence results in high gain and UGB of the OTA. Moreover, simulation of the bulk-driven quasi-floating gate OTA does not suffer from DC convergence problem. A voltage mode multifunction 2nd order filter design based on proposed BDQFG OTA is also presented. The analysis of all the circuits have been carried out in industry specific node UMC 0.18 micron technology with the help of HSpice simulator.

KEYWORDS

Bulk driven, Bulk driven QFG, Transconductance, Bandwidth, OTA, filter

1. INTRODUCTION

The design of low power, low cost and maintenance free medical equipments has become essential for long-term monitoring applications implemented in deep submicron technologies. The downscaling of CMOS technology in nanometre regime is easily accomplished in digital circuits but not so easily adopted for analog circuits. The short channel effect resulting in offset and decreased output impedance are serious issues in the design of analog circuits. The scaling down of supply voltage for achieving low power dissipation also has the limitation that threshold voltage of a MOS transistor is not scalable [1]. Many circuit design techniques such as bulk-driven (BD), sub-threshold operation, level shifter, floating-gate (FG) and quasi-floating gate (QFG) have been reported to achieve low power dissipation [2-4]. The design of OTA [5], op-amp [6, 7], linearized OTA for bio-medical application [8, 9], self-biased cascode current mirror [10] etc using bulk-driven technique have been reported in literature.

Even though the bulk driven technique have been used in the design of various circuits due to its simple architecture the technique suffers from low gain due to body transconductance and also its large sensitivity to device mismatch and process variations. To increase the effective transconductance partial positive feedback at input stage has been employed [11, 12]. However due to the sensitivity of bulk-driven circuits to device mismatch and process variation the positive feedback results in reduced stability and also degrades the frequency response. The wide band QFG transistor based circuits operating at low supply voltage have been reported [13]. A combination of BD and QFG techniques has been reported recently (BDQFG) [14]. The circuits realized using this technique offer larger transconductance and bandwidth as compared to the BD and QFG based circuits. The capacitive voltage divider network used at gate input in QFG

transistors results in improved linearity of QFG transistor. This feature of QFG MOS transistor has been used in the design of highly linear programmable CMOS OTA [15], tunable MOS resistor [16], GM-C filter [17], current conveyor [18], current mirror [19, 20] etc. The experimental verification has proved the QFG to be a better choice for the design of low voltage low power circuits [13]. Though QFG MOST has several advantages the DC convergence has still been an issue since the currently available spice simulators do not converge for capacitive networks for DC analysis. The use of BDQFG transistor DC convergence problem does not arise because under DC conditions the transistor works as simple BD while under AC conditions the transistor works as BDQFG.

The paper presents two-stage miller compensated OTA designed with BDQFG MOS transistors. The performance of the proposed OTA is compared with conventional miller OTA designed with BD transistors. A voltage mode multifunction 2nd order filter using the proposed miller compensated OTA has been designed. The simulation results indicate that the BDQFG is a better option for high frequency low power applications. The paper is organized as follows: section 2 of the paper presents a brief discussion on BDQFG MOSFET followed by the analysis of BDQFG based miller compensated OTA in section 3. The design of the multifunction filter has been presented in section 4. The simulations results for the proposed OTA and the filter circuit have been presented in section 5. The paper is concluded in section 6.

2. BDQFG MOSFET

The conventional MOS transistor is a four terminal device whose bulk terminal is usually connected to the most negative/positive supply voltage for N-channel/P-channel MOS transistor respectively. If the signal input is applied to the bulk terminal the signal amplitude need not be larger than the threshold voltage in the transistor as required in case of gate input circuits. Therefore in this mode the input signal is not constrained by the threshold voltage limitation and even very low amplitude signals can be used at the bulk input. Based on this, BD technique was first reported in [21]. The operation of the transistor in this mode is similar to that of a junction field effect transistor (JFET). The schematic of BD technique is shown in Fig. 1 (a). The dc bias voltage V_{bias} applied at gate creates the channel whereas the input applied at bulk modulates the drain-to-source current even with very small amplitude of input signal. The most significant drawback related to the bulk-driven MOS transistor is its small body transconductance (g_{mb}) and degraded frequency response [22]. The body transconductance (g_{mb}) is related to gate transconductance (g_m) as

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}} g_m = \eta g_m \quad (1)$$

where γ is the body effect co-efficient, ϕ_f is the fermi-potential, and V_{SB} is the source-to-bulk potential. The normal range of η varies from 0.2 to 0.4. The low transconductance results in poor open-loop gain and bandwidth. As discussed, BDQFG offer significant advantages over BD. The schematic of BDQFG MOSFET is shown in fig. 1 (b) where the bulk is tied to the gate input terminal of QFG MOS transistor M1. Under DC analysis it works as simple BD MOST whereas for AC analysis it combines the effect of BD and QFG MOS transistors. The result is an improved frequency response. The BDQFG MOS transistor has been used in the design of differential difference current conveyor [23], high bandwidth self-cascode current mirror [24]. A recent research paper [25] has reported experimental evidence of using BDQFG for realizing low power circuits.

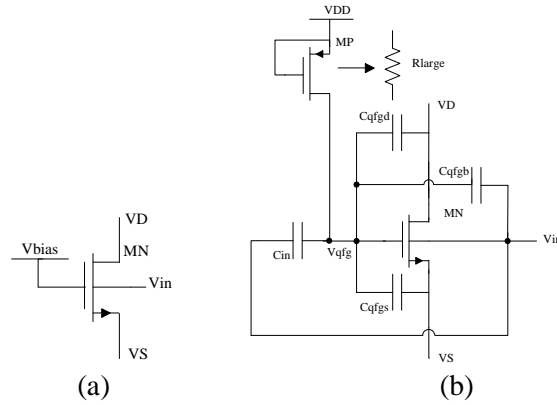


Figure 1. N-Channel: (a) BD, and (b) BD-QFG MOS transistor

3. PROPOSED MILLER OTA

OTA is the voltage-controlled current source device, used as versatile building blocks which offer wide bandwidth for many types of amplifiers. The ideal characteristics of OTA are high bandwidth and high input and output impedances. The conventional bulk driven OTA as discussed in literature has limited linearity, low gain and bandwidth. The conventional bulk-driven miller compensated OTA referred in this paper is shown in Fig. 2 [26]. The combination (M3, M4) and (M5, M6, M7) are simple current mirror architectures. The MOS transistor M5, M6 and M7 is also used for providing the biasing current (I_{bias}) to various branches of the amplifier. The miller compensation is done via C_c which improve the phase response of two-stage amplifier. But due to feed forward path via miller capacitor a zero is created in right half plane which degrades the phase shift of amplifier and cause stability issues at high frequency. In order to reduce the zero effect a nulling resistor (R_c) is used in series with miller capacitor. The use R_c introduces an extra pole and its appropriate selection cancels the zero effect preventing instability issues at high frequency. Though the differential pair being used in bulk-driven consumes low power the OTA has poor gain and low bandwidth due to body transconductance of input MOST. In context to this, the BDQFG technique solves the BD body transconductance by boosting it by transconductance of QFG MOST i.e. $g_{m,BDQFG} = g_{mb} + g_{m,QFG}$. Based on BDQFG technique the schematic of proposed miller compensated OTA is shown in Fig. 3. The proposed OTA uses BDQFG input differential pair which results in enhanced transconductance of OTA and also improved UGB product.

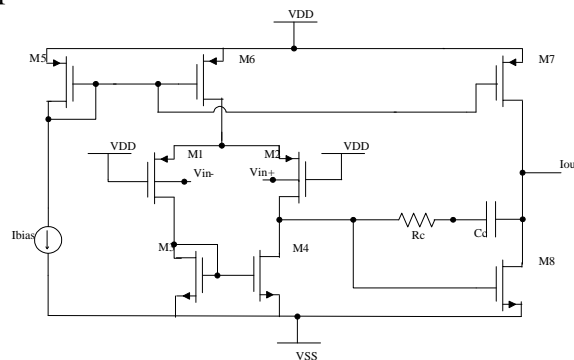


Figure 2. Conventional BD Miller compensated OTA

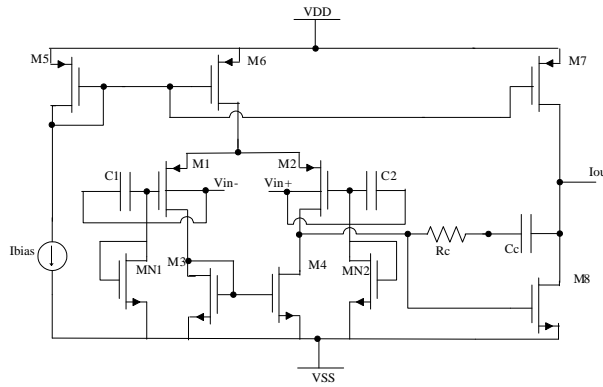


Figure 3. Proposed BDQFG Miller compensated OTA

The equations for current, transconductance and output resistance of saturation mode N-channel/P-channel MOS transistor are given as

(i) Drain-to-source current:

(ii)

$$I_{DSsat} = \frac{1}{2} \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) V_{eff,n,p}^2 \quad (2)$$

(ii) Transconductance:

$$g_m = \sqrt{2 \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) I_{DSsat}} \quad (3)$$

(iii) Output resistance

$$r_0 = 1/\lambda I_{DSsat} \quad (4)$$

where $V_{eff,n} = V_{GS} - V_{th,n}$, $V_{eff,p} = V_{SG} - |V_{th,p}|$. Assume all the MOS transistors used for OTA design in Fig. 2 and Fig. 3 are operating in saturation region except MN1 and MN2 of Fig. 3. The small-signal model for calculating transconductance of proposed miller compensated OTA is shown in Fig. 4.

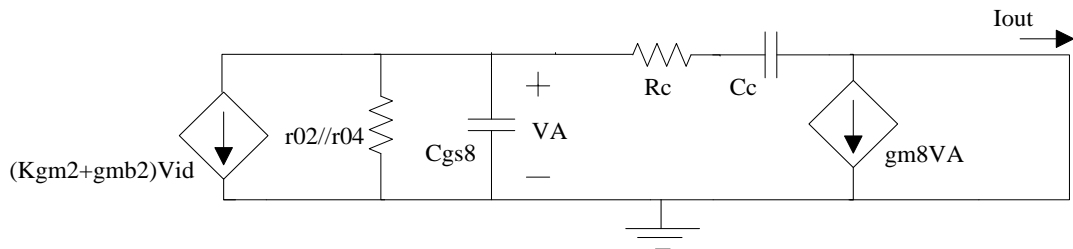


Figure 4. Small-signal model for calculating transconductance of proposed OTA

At input

$$(kg_{m2} + g_{mb2})V_{id} + \frac{V_A}{r_{02} // r_{04}} + sC_{gs6}V_A + \frac{sC_c}{1 + sR_c C_c}V_A = 0 \quad (5)$$

Solving for V_A

$$V_A = - \frac{(kg_{m2} + g_{mb2})(r_{02} // r_{04})(1 + sR_C C_C)}{1 + (R_C C_C + (r_{02} // r_{04})(C_{gs6} + C_C))s + ((r_{02} // r_{04})R_C C_{gs6} C_C)s^2} V_{id} \quad (6)$$

At output

$$I_{out} = \frac{sC_C}{1 + sR_C C_C} V_A - g_{m8} V_A \quad (7)$$

Putting (6) in (7)

$$I_{out} = - \frac{(kg_{m2} + g_{mb2})(r_{02} // r_{04})(sC_C - g_{m8}(1 + sR_C C_C))}{1 + (R_C C_C + (r_{02} // r_{04})(C_{gs6} + C_C))s + ((r_{02} // r_{04})R_C C_{gs6} C_C)s^2} V_{id} \quad (8)$$

$$G_{m,proposed} = \frac{I_{out}}{V_{id}} = - \frac{(kg_{m2} + g_{mb2})(r_{02} // r_{04})(1 - g_{m8}R_C)C_C \left(s - \frac{g_{m8}}{C_C(1 - g_{m8}R_C)} \right)}{1 + (R_C C_C + (r_{02} // r_{04})(C_{gs6} + C_C))s + ((r_{02} // r_{04})R_C C_{gs6} C_C)s^2} \quad (9)$$

Rearranging (9)

$$G_{m,proposed} = - \frac{\left(\frac{(kg_{m2} + g_{mb2})(1 - g_{m8}R_C)}{R_C C_{gs6}} \right) \left(s - \frac{g_{m8}}{C_C(1 - g_{m8}R_C)} \right)}{s^2 + \left(\frac{1}{(r_{02} // r_{04})C_{gs6}} + \frac{(C_{gs6} + C_C)}{R_C C_{gs6} C_C} \right) s + \frac{1}{(r_{02} // r_{04})R_C C_{gs6} C_C}} \quad (10)$$

At $s = 0$, the transconductance of OTA is calculated to be

$$G_{m,proposed} = (kg_{m2} + g_{mb2})g_{m8}(r_{02} // r_{04}) \quad (11)$$

While for BD OTA (Fig. 2)

$$G_{m,BD} = g_{mb2}g_{m8}(r_{02} // r_{04}) \quad (12)$$

As seen from (11) the increased transconductance of 1st stage results in enhanced transconductance of OTA. The end result of other analytical analysis for referred and proposed OTA is shown in following equations:

3.2 Output Resistance

The output resistance is estimated by the equation

$$R_{out,proposed} = R_{out,BD} = (r_{07} // r_{08}) \quad (13)$$

Since 2nd stage is identical so no change in output resistance is observed.

3.3 DC Gain

The gain of the OTA is given by

$$A_{0,proposed} = (kg_{m2} + g_{mb2})g_{m8}(r_{02} // r_{04})(r_{07} // r_{08}) \quad (14)$$

While for BD OTA

$$A_{0,BD} = g_{mb2}g_{m8}(r_{02} \parallel r_{04})(r_{07} \parallel r_{08}) \quad (15)$$

From (14) an increment in gain can be observed as due to enhanced transconductance of BDQFG MOSFET M2.

3.4 Dominant pole

The -3db frequency is given by

$$\omega_{p1,proposed} \approx \omega_{p1,BD} \cong \frac{1}{g_{m8}(r_{02} \parallel r_{04})(r_{07} \parallel r_{08})C_c} \quad (16)$$

No changes occur in dominant pole location as the output stage is identical for both the OTA.

3.5 Unity-gain bandwidth (UGB)

The UGB product is given by

$$UGB(\omega_{u,proposed}) \cong A_{0,proposed}\omega_{p1,proposed} \approx \frac{(kg_{m2} + g_{mb2})}{C_c} \quad (17)$$

While for BD OTA

$$UGB(\omega_{u,BD}) \cong A_{0,BD}\omega_{p1,BD} \approx \frac{g_{mb2}}{C_c} \quad (18)$$

The improved gain of BDQFG OTA results in high UGB product as observed in (14). In summary, the proposed BDQFG OTA provides high gain and better UGB product as compared to BD OTA and maintains the same level of power consumption.

4. VOLTAGE MODE 2ND ORDER MULTIFUNCTION FILTER USING PROPOSED BDQFG OTA

The architecture of 2nd order transconductor-capacitor ($G_m - C$) voltage mode multifunction filter [27] realization based on proposed OTA (Fig. 3) is shown in Fig. 5. The two OTA used are labelled as G_{m1} and G_{m2} along with two external capacitors c_1 and c_2 to realize low pass (LP), band pass (BP), and high pass (HP) filter.

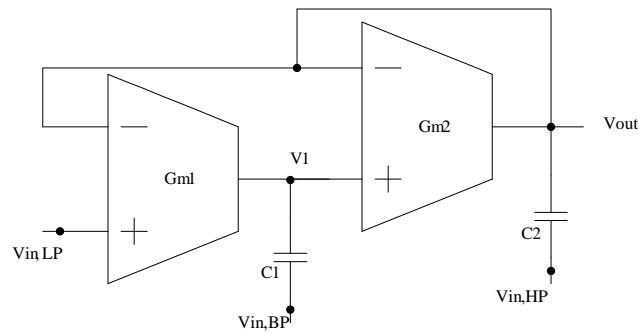


Figure 5. Voltage mode Multifunction 2nd order filter using proposed OTA

For 1st OTA,

$$G_{m1} = \frac{sC_1(V_1 - V_{in,BP})}{V_{in,LP} - V_{out}} \quad (19)$$

For 2nd OTA

$$G_{m2} = \frac{sC_2(V_{out} - V_{in,HP})}{V_1 - V_{out}} \quad (20)$$

From (20) solving for v_1

$$V_1 = \left(1 + \frac{sC_2}{G_{m2}} \right) V_{out} - \frac{sC_2}{G_{m2}} V_{in,HP} \quad (21)$$

Putting (21) in (19) yields the output as

$$V_{out} = \frac{s^2 V_{in,HP} + \left(\frac{1}{C_2} \right) s V_{in,BP} + \frac{G_{m1}}{C_1 C_2} V_{in,LP}}{s^2 + \left(\frac{G_{m2}}{C_2} \right) s + \frac{G_{m1} G_{m2}}{C_1 C_2}} \quad (22)$$

Hence, from (22) the -3dB frequency and the quality factor is calculated as

$$\omega_0 = \sqrt{\frac{G_{m1} G_{m2}}{C_1 C_2}} \quad (23)$$

And

$$Q = \sqrt{\frac{G_{m1} C_2}{G_{m2} C_1}} \quad (24)$$

To realise the filtering responses three conditions arises as:

Case (i): when $V_{in,BP} = V_{in,HP} = 0$ the architecture performs 2nd order low pass filtering and the transfer function is given as

$$\frac{V_{out}}{V_{in,LP}} = \frac{G_{m1}/C_1 C_2}{s^2 + (G_{m2}/C_2)s + (G_{m1}G_{m2}/C_1 C_2)} \quad (25)$$

Case (ii): when $V_{in,LP} = V_{in,HP} = 0$ the architecture performs 2nd order band pass filtering and the transfer function is given as

$$\frac{V_{out}}{V_{in,BP}} = \frac{(1/C_2)s}{s^2 + (G_{m2}/C_2)s + (G_{m1}G_{m2}/C_1 C_2)} \quad (26)$$

Case (iii): when $V_{in,LP} = V_{in,BP} = 0$ the architecture performs 2nd order high pass filtering and the transfer function is given as

$$\frac{V_{out}}{V_{in,HP}} = \frac{s^2}{s^2 + (G_{m2}/C_2)s + (G_{m1}G_{m2}/C_1 C_2)} \quad (27)$$

5. SIMULATION RESULTS

The miller compensated OTA of Fig. 2 and Fig. 3 and filter of Fig. 4 has been simulated on 0.18 μm mixed-mode twin-well technology provided by UMC with the help of HSpice simulator. The dimensions of MOS transistors used for OTA realisation of Fig. 2 and Fig. 3 is shown in table 1. The values of other parameters assumed for OTA are also listed in table 1.

Table 1. Dimension of MOS transistors used in Miller OTA

MOSFET	W (μm)	L (μm)	MOSFET	W (μm)	L (μm)
M1	12	0.6	M6	9	0.6
M2	12	0.6	M7	8	0.6
M3	12	0.6	M8	23.9	0.6
M4	12	0.6	MP1	0.24	0.24
M5	4	0.6	MP2	0.24	0.24
$R_c = 10K, C_c = 1pf, C_1 = C_2 = 1pf, C_{load} = 1pf, I_{bias} = 10 \mu A$					

The plot of effective transconductance of referred and proposed OTA is shown in Fig. 6. From the plots it can be observed that for BD configuration the transconductance is very low whereas this is not the case with the BDQFG based OTA. The proposed OTA shows boosted transconductance by fourfold due to added transconductance of QFG MOS transistor with BD MOS transistor. This increased transconductance reflects in gain enhancement by 14dB over conventional BD OTA as shown in Fig. 7. As there is no significant impact on output impedance and so no change in -3db frequency is observed. The effect of high transconductance is also reflected in UGB product which on simulation is found to be enhanced by nine times over BD OTA maintaining the same level of power consumption. The output response for input step signal is observed by performing transient analysis shown in Fig. 8.

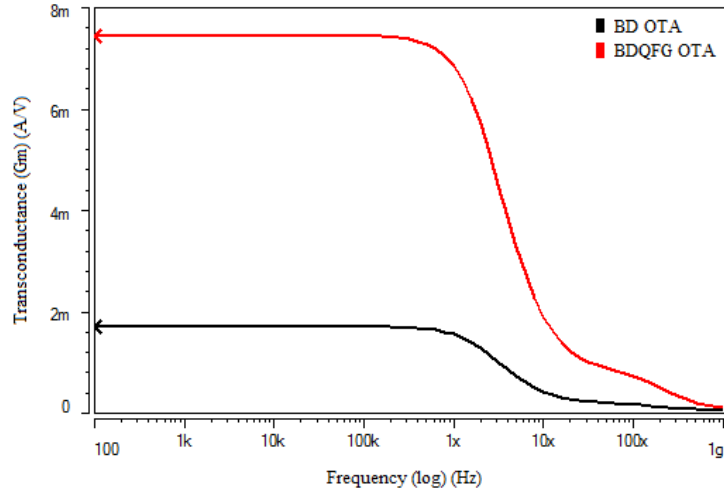


Figure 6. Transconductance of BD and proposed OTA

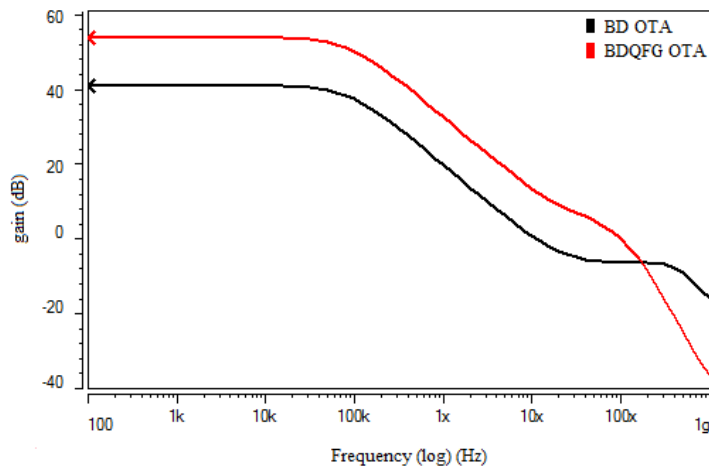


Figure 7. Frequency response of BD and proposed OTA

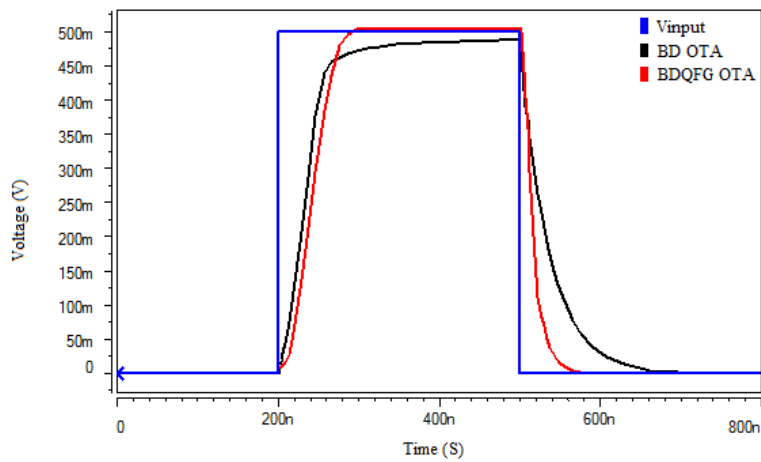


Figure 8. Transient response of BD and proposed OTA

From simulation results, it can be concluded that BDQFG is a better option for realizing high gain circuits with low power consumption. The simulation results value has been tabulated in table 2.

Table 2. Comparative analysis of BD and BDQFG OTA

Parameters	BD OTA	Proposed BDQFG OTA
Transconductance (G_m) ($\mu A/V$)	1700	7440
DC gain	40.9	53.81
Dominant pole (KHz)	87.8	87.1
UGB (MHz)	11.27	101.13
Phase Margin (PM)	114	65
Power (μW)	51.47	51.46
Output impedance ($K\Omega$)	117	117
Rise time (nS)	53.94	51.28
Fall time (nS)	76.20	28.35
Voltage Supply	$\pm 0.5V$	$\pm 0.5V$

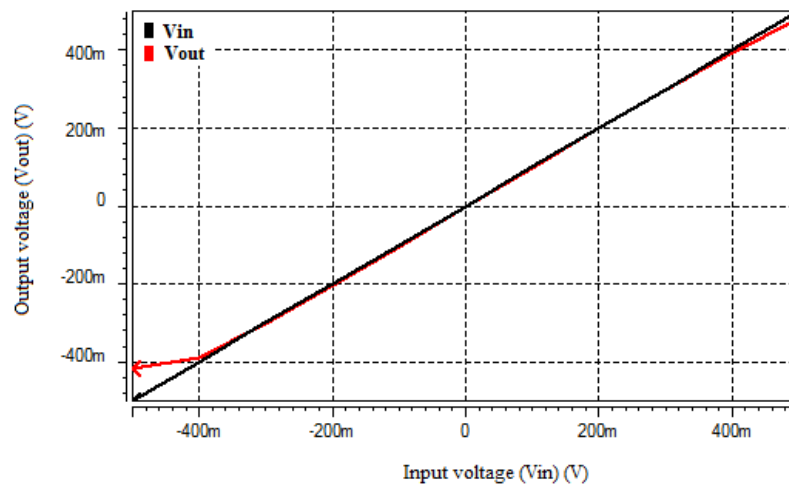


Fig. 9 DC analysis for input voltage swept from -500mV to 500mV

Further simulation results are shown for voltage mode 2nd order multifunction filter of Fig. 5. The filter is designed for 1 KHz cut-off frequency. The DC analysis result shown in Fig. 9 proves the linear range of filter to its supply rails. The simulation has been performed for input voltage swept from -500mV to 500mV at the steps of 100mV. The magnitude and phase responses for LP, BP and HP filter is shown in Fig. 10 and Fig. 11 respectively.

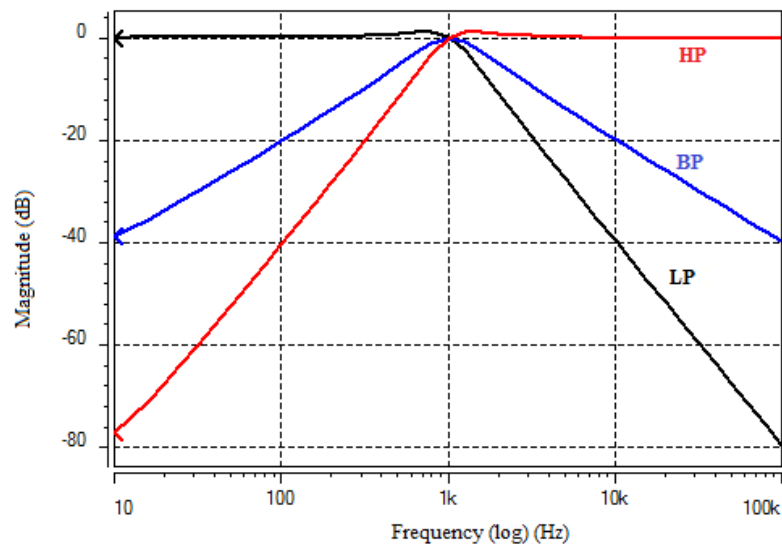


Figure 10. Simulated magnitude plot of LP, BP and HP filter responses

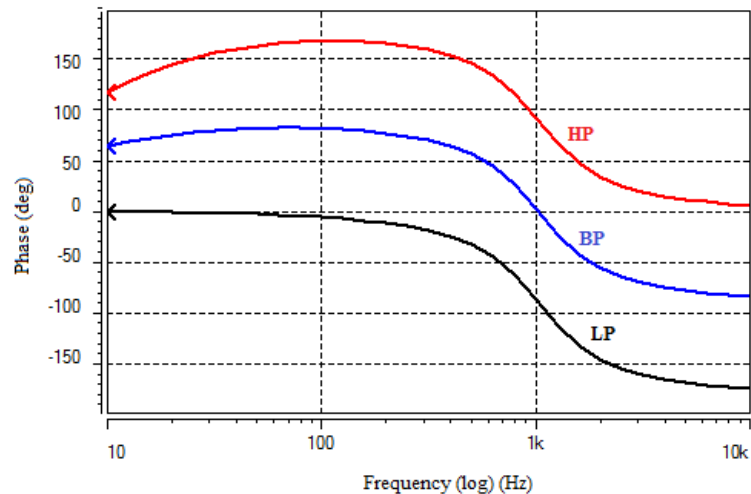


Figure 11. Simulated phase plot of LP, BP and HP filter responses

6. CONCLUSIONS

In this paper, performance analysis of miller compensated OTA based on BD and BDQFG by simulations is presented. It has been shown that BDQFG technique offers significant advantage over BD based OTA in terms of transconductance and UGB product. Further an application of proposed OTA is shown in realisation of voltage mode 2nd order multifunction filter. All the circuits have been implemented / simulated using UMC 0.18 μm twin-well process through HSpice simulator.

REFERENCES

- [1] Blalock, B. J.; Allen, P. E.; & Rincon-Mora, G. A.; "Designing 1-V op amps using standard digital CMOS technology", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 769-780, 1998. (<http://dx.doi.org/10.1109/82.700924>)
- [2] Khateb, F.; Dabbous, S.B.A. & Vlassis, S. "A survey of non-conventional techniques for low-voltage low-power analog circuit design", *Radioengineering*, vol. 22, no. 2, pp. 415-427, 2013.
- [3] Raj, N.; Singh, A.K.; & Gupta, A.K. "Low Power Circuit Design Techniques: A Survey", *International Journal of Computer Theory and Engineering*, vol. 7, no. 3, pp. 172-176, 2015. (<http://dx.doi.org/10.7763/IJCTE.2015.V7.951>)
- [4] Raj, N. & Gupta, A.K. "Analysis of Operational Transconductance Amplifier using Low Power Techniques", *Journal of Semiconductor Devices and Circuits*, vol. 1, no. 3, pp. 1-9, 2015.
- [5] Khameh, H. & Shamsi, H. "On the design of a low-voltage two stage OTA using bulk-driven and positive feedback techniques", *International Journal of Electronics*, vol. 99, no. 9, pp. 1309-1315, 2012. (<http://dx.doi.org/10.1080/00207217.2012.669710>)
- [6] Stockstad, T. & Yoshizawa H. "A 0.9-V 0.5 μ A rail-to-rail CMOS operational amplifier", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 286-292, 2002. (<http://dx.doi.org/10.1109/4.987079>)
- [7] Zuo, L. & Islam S.K. "Low-Voltage Bulk-Driven Operational Amplifier with Improved Transconductance", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 8, pp. 2084-2091, 2013. (<http://dx.doi.org/10.1109/TCSI.2013.2239161>)
- [8] Raj N. & Sharma R.K. "Modeling of Human Voice Box in VLSI for Low Power Biomedical Applications", *IETE Journal of Research*, vol. 57, no. 4, pp. 345-353, 2011. (<http://dx.doi.org/10.4103/0377-2063.86337>)
- [9] Gak, J.; Miguez, M.R. & Arnaud, A. "Nanopower OTAs with Improved Linearity and Low Input Offset Using Bulk Degeneration", *IEEE Transactions on Circuits and Systems I: Regular Papers*, No. 99, pp.1-10, 2013. (<http://dx.doi.org/10.1109/TCSI.2013.2284002>)
- [10] Aggarwal, B.; Gupta, M. & Gupta A.K. "Analysis of low voltage bulk-driven self-biased high swing cascode current mirror", *Microelectronics Journal*, Vol. 44, No. 3, pp. 225-235, 2013. (<http://dx.doi.org/10.1016/j.mejo.2012.12.006>)
- [11] Carrillo, J.M.; Torelli, G.; Pérez-Aloe, R. & Duque-Carrillo, J.F. "1-V rail-to-rail CMOS op-amp with improved bulk-driven input stage", *IEEE Journal of Solid State Circuits*, vol. 42, no. 3, pp. 508-517, 2007. (<http://dx.doi.org/10.1109/JSSC.2006.891717>)
- [12] Raikos, G. & Vlassis, S. "Low-voltage bulk-driven input stage with improved transconductance", *International Journal of Circuit Theory and Application*, vol. 39, no. 3, pp. 327-339, 2011. (<http://dx.doi.org/10.1002/cta.637>)
- [13] Ramirez-Angulo, J.; Lopez-Martin, A.J.; Gonzalez-Carvajal, R. & Munoz Chavero, F. "Very low voltage analog signal processing based on quasi floating gate transistors", *IEEE Journal of Solid State Circuits*, Vol. 39, pp. 434-442, 2004. (<http://dx.doi.org/10.1109/JSSC.2003.822782>)
- [14] Khateb, F. "Bulk-driven floating-gate and bulk-driven quasi-floating-gate techniques for low-voltage low-power analog circuits design", *AEU-International Journal of Electronics and Communications*, Vol. 68, No. 1, pp. 64-72, 2013. (<http://dx.doi.org/10.1016/j.aeue.2013.08.019>)
- [15] Miguel, J. M. A.; Lopez-Martin, A. J.; Acosta, L.; Ramirez-Angulo, J. & Carvajal, R. G. "Using Floating Gate and Quasi-Floating Gate Techniques for Rail-to-Rail Tunable CMOS Transconductor Design", *IEEE Transaction on Circuits and Systems I: Regular Papers*, Vol. 58, No. 7, pp. 1604-1614, 2011. (<http://dx.doi.org/10.1109/TCSI.2011.2157782>)
- [16] Torralba, A.; Luján-Martínez, C.; Carvajal, R.G.; Galan, J.; Pennisi, M.; Ramirez-Angulo J. & López-Martin, A. "Tunable Linear MOS Resistors Using Quasi-Floating-Gate Techniques", *IEEE Transaction on Circuits and Systems II: Express Briefs*, Vol. 56, No. 1, pp. 41-45, 2009. (<http://dx.doi.org/10.1109/TCSI.2008.2010163>)
- [17] Garcia-Alberdi, C.; Lopez-Martin, A.; Acosta, L.; Carvajal, R.G. & Ramirez-Angulo, J. "Tunable Class AB CMOS Gm-C Filter Based on Quasi-Floating Gate Techniques", *IEEE Transaction on Circuits and Systems I: Regular Papers*, Vol. 60, No. 5, pp. 1300-1309, 2013. (<http://dx.doi.org/10.1109/TCSI.2012.2220504>)
- [18] Moradzadeh, H. & Azhari, S. J. "Low-voltage low-power rail-to-rail low-Rx wideband second generation current conveyor and a single resistance-controlled oscillator based on it", *IET Circuits, Devices & Systems*, Vol. 5, No. 1, pp. 66-72, 2011. (<http://dx.doi.org/10.1049/iet-cds.2010.0178>)

- [19] Gupta, R. & Sharma, S. "Quasi-floating gate MOSFET based low voltage current mirror", *Microelectronics Journal*, 2012, Vol. 43, No. 7, pp. 439-443, 2012. (<http://dx.doi.org/10.1016/j.mejo.2012.04.006>)
- [20] Raj, N.; Singh, A.K. & Gupta, A.K. "Low power high output impedance high bandwidth QFGMOS current mirror", *Microelectronics Journal*, vol. 45, no. 8, pp. 1132-1142, 2014. (<http://dx.doi.org/10.1016/j.mejo.2014.05.005>)
- [21] Guzinski, A.; Bialko, M. & Matheau, J.C. "Body driven differential amplifier for application in continuous-time active C-filter", in *Proc. ECCD, 1987*, Paris, France, 1987, pp. 315-319.
- [22] Rosenfeld, J.; Kozak, M. & Friedman, E.G. "A bulk-driven CMOS OTA with 68 dB DC gain", in *Proc. of the 11th IEEE International Conference on Electronics, Circuits and Systems*, 2004, pp. 5-8. (<http://dx.doi.org/10.1109/ICECS.2004.1399600>)
- [23] Khateb, F.; Jaikl, W.; Kumngern, M. & Prommee, P. "Comparative study of sub-volt differential difference current conveyors", *Microelectronics Journal*, vol. 44, no. 12, pp. 1278-1284, 2013. (<http://dx.doi.org/10.1016/j.mejo.2013.08.015>)
- [24] Raj, N.; Singh, A.K. & Gupta, A.K. "Low-voltage bulk-driven self-biased cascode current mirror with bandwidth enhancement", *Electronics Letters*, Vol. 50, No. 1, pp. 23-25, 2014. (<http://dx.doi.org/10.1049/el.2013.3600>)
- [25] Khateb, F. "The experimental results of the bulk-driven quasi-floating-gate MOS transistor", *AEU - International Journal of Electronics and Communications*, vol. 69, no. 1, pp. 462-466, 2015. (<http://dx.doi.org/10.1016/j.aeue.2014.10.016>)
- [26] Allen, P. E. & Holberg D.R. *CMOS Analog Circuit Design*, Oxford University Press, 2002, USA.
- [27] Khateb, F.; Khatib, N.; Prommee, P.; Jaikla, W. & Fucjik, L. "Ultra-low voltage tunable transconductor based on bulk-driven quasi-floating-gate technique", *Journal of Circuit, System, and Computer*, vol. 22, pp. 1-13, 2013. (<http://dx.doi.org/10.1142/S0218126613500734>)

AUTHORS

Nikhil Raj received B.E. (ECE) from Dr. B.A.M.U. Maharashtra in 2005. He received his M.Tech (VLSI Design) from National Institute of Technology, Kurukshetra in the year 2010. He served as Assistant Professor at NIT Kurukshetra during the period 2009-11. Since 2011, he is with National Institute of Technology, Kurukshetra where he is presently research scholar. He has also served in the capacity of Research Assistant at Curtin University, Sarawak, Malaysia during the period 2013-14. His areas of interest are Low power, bio-inspired circuits.



Anil Kumar Gupta received B.Tech (ECE) from G.B. Pant University of Agriculture and Technology in 1972. He received M.Tech and Ph.D in Electrical Engineering from Indian Institute of Technology, Kanpur in the years 1974 and 1985 respectively. He served as Assistant Station Engineer in All India Radio during the period 1974-78. Since 1985, he is with NIT Kurukshetra where he is presently serving as Professor, Electronics and Communication Engineering for the last thirteen years. His areas of interest are Semiconductor devices and Technology, Embedded systems, VLSI Design.

