AN ENHANCED LOW POWER HIGH PSRR BAND GAP VOLTAGE REFERENCE USING MOSFETS IN STRONG INVERSION REGION

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ABSTRACT

In this paper, a band gap voltage reference using MOSFETs in strong inversion region is presented. The proposed circuit represents a high PSRR (Power Supply Rejection Ratio) and low temperature sensitivity and is capable of operating properly at supply voltages lower than 1v. In the designed circuit, the PSRR is improved using regulated voltage and a feedback loop. In addition, the circuit is independent on supply voltage noise. The circuit is designed in 180nm TSMC CMOS technology and is simulated using HSPICE. The obtained output voltage is 466.7mV and the obtained temperature deviation average under temperatures between -20°c to 100°c is 29.1 ppm/c°. PSRR is 109 dB at low frequencies. Calculated power dissipation with 1.2v supply voltage in room temperature is 42μw.

KEYWORDS

Band Gap Voltage Reference, Temperature Sensitivity, PSRR, Strong Inversion.

1. INTRODUCTION

Band gap voltage reference is one of the most important blocks in many analog and digital systems, e.g., Analog to Digital and Digital to Analog Converters. In band gap voltage references, low temperature coefficient and high PSRR are strongly desired. Meanwhile, the voltage reference should provide low power dissipation and must be capable of operating properly at low supply voltages. Numerous types of voltage references and temperature sensors have been designed by means of Bipolar Junction Transistors (BJTs) due to their desired temperature features[1-2]. In fact, in most of the previous works, unequal current density of two BJTs is employed to generate a difference in Base Emitter voltage of the two transistors, making the Base-Emitter voltage of the two transistors (ΔVBE) is directly proportional to temperature. On the other hand, it is known that the Base-Emitter voltage(VBE) is inversely proportional to temperature. HenceIn most band gap voltage reference circuits it is desired to sum up ΔVBE and

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VBE in order to obtain a temperature-independent voltage reference. However, the aimed voltage reference might be practically challenging to obtain due to non-linear variations of VBE with temperature [3-5].

In this paper, a new technique is presented in order to address this problem. MOSFETs in strong inversion region are used in the place of BJTs. Furthermore, a regulated and improved current structure is used in order to obtain a high PSRR.Firstly, the proposed circuit is analysed. Afterwards, a feedback loop is inserted between the regulated voltage node and the operational amplifier. Utilizing the regulated voltage and the feedback loop leads toan improved PSRR. At last, the simulation results and conclusion are presented. [12]

2. THE PROPOSED BAND GAP VOLTAGE REFERENCE

The Gate-Source voltage of NMOS transistors depends on electron mobility and threshold voltage, which is described in (1).

$$V_{GS} = V_{tn} + \sqrt{\frac{2LI_D}{C_{OX}W\mu_n}} \tag{1}$$

Where I_D is the drain current of the transistor, W/L is the width-to-length ratio of the channel and Cox is unit capacitor of the Gate-Oxide. μ_n is the electron mobility and V_{th} is the threshold voltage of N MOS transistor. The threshold voltage and electrons mobility dependence on temperature are given in (2) and (3) as mentioned in [6].

$$\mu_n(T) = \mu_{n0}\left(\frac{T}{T_0}\right)^{\propto_{\mu n}} \tag{2}$$

$$V_{tn} = V_{tno} + \propto_{vtn}(T - T_0) \tag{3}$$

where μ_{n0},$\propto_{\mu n}$,$\propto_{vtn}$,V_{tno} are constant values and $\propto_{\mu n}$,$\propto_{vtn}$ are negative constants. T_0 and T are 300 kelvin and temperature coefficient, respectively. $\alpha_{\mu n}$ in equation (2) ranges between -1 and -2. Therefore, the electron's mobility is inversely proportional to temperature. Since α_{vth} in equation (3) is negative, threshold voltage of NMOS is inversely proportional to temperature. The Gate-Source voltage of NMOS in equation(1) is capable of varying both inversely and directly with temperature. The first term produces the inverse relationship and the produces the direct relationship with temperature in VGS.

Equation (4) shows variations of resistance with temperature. This phenomenon strongly affects both directly and inversely temperature-dependent currents in band gap voltage references and cause significant changes in the mentioned currents. The amount of resistance in the ambient temperature T_0 is shown as $R(T_0)$bellow, which is dependent on fabrication process. However, temperature coefficients of $T_{C1}$and $T_{C2}$are constant values and are independent on fabrication process.

$$R(T) = R(T_0)[1 + TC_1(T - T_0) + TC_2(T - T_0)^2] \tag{4}$$

Thus, a resistor with smaller temperature coefficient is required. Consequently, unsolicited Poly silicon resistor in 180nm CMOS technology is utilized in the proposed circuit.

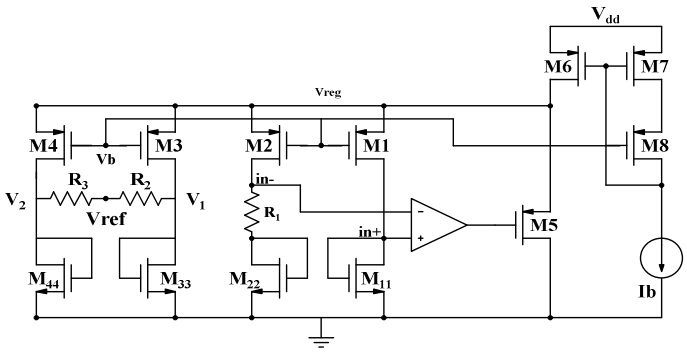

Figure 1. General schematic of proposed band gap reference

The structure of a band gap voltage reference using bipolar transistors with high PSRR is illustrated in fig.1. [7]. PSRR is improved in the circuit using regulated voltage of VREG. In this structure, regulated voltage and supply voltage have been separated. In contrast with the previously suggested band gap voltage references, the required decrease in supply voltage is equal to Source-Drain voltage in M6 and M7 transistors. In continue, the structure of the proposed band gap voltage reference using diode MOSFETs in strong inversion region is demonstrated in Fig. 2. +in and –in nodes in operational amplifier are equal. The voltage across R_1 varies with temperature according to equations (5) and (6). Temperature behaviour of Gate Source voltage in diode transistors depend on the drain current and the size of the NMOS transistor.

$$V_{R1} = V_{GS11} - V_{GS22} \tag{5}$$

$$V_{R1} = V_{tn11} + \sqrt{\left(\frac{2LI_D}{C_{OX} W\mu_n}\right) M_{11}} - V_{tn22} - \sqrt{\left(\frac{2LI_D}{C_{OX} W\mu_n}\right) M_{22}} \tag{6}$$

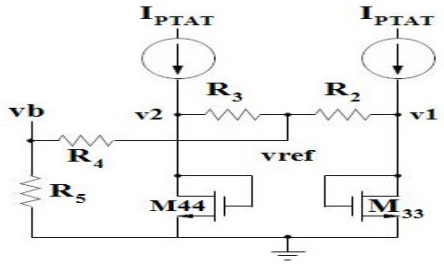

Figure 2.Output voltage circuit for proposed band gap reference

Channel length and drain current of M11 and M22 of equation (6) are equal and their threshold voltages are close. Hence, equation (6) can be simplified as equation (7)

$$V_{R1} = \sqrt{\left(\frac{2LI_D}{C_{OX}\,W\mu_n}\right)M_{11}} - \sqrt{\left(\frac{2LI_D}{C_{OX}\,W\mu_n}\right)M_{22}} \quad (7)$$

VR1 in equation (7) is subtraction of two temperature-dependent terms. In order to obtain variations in voltage across R1 which is proportional to temperature, first term must be greater than the latter. Consequently, using proper values for channel length in M11 and M22 diode transistors result in proportionally temperature-dependent voltage across R1. In other words, W22 must be greater than W11 and it must be W22=1.39W11.

Current flowing through R1 resistor is calculated from equation (8). The current is obtained as a result of the difference in Gate-Source voltages of M11 and M22 across R1. Equation (9) suggests that the current flowing through M3 and M4 are proportional to IR1.

$$I_{R1} = \frac{V_{GS11} - V_{GS22}}{R_1} = \frac{\Delta V_{GS}}{R_1} \quad (8)$$

$$I_{M3,4} = I_{R1}\left(\frac{(W/L)_{M3,4}}{(W/L)_{M1,2}}\right) \quad (9)$$

Voltages of V1 and V2 nodes are the Gate-Source voltages of M33 and M44, respectively, which are diode connected in strong inversion region. The output voltages before connecting R4 and R5 is calculated from equation (10).

$$v_{ref} = \frac{V_{GS33}}{1+(R_2/R_3)} + \frac{V_{GS44}}{1+(R_3/R_2)} \quad (10)$$

Equation (10) is more precisely expressed in equation (11). R2 and R3 are equal and do not have any effect on output temperature behaviour.

$$v_{ref} = \frac{V_{tn33} + \sqrt{\left(\frac{2LI_D}{C_{OX}\,W\mu_n}\right)_{M33}}}{1+(R_2/R_3)} + \frac{V_{tn44} + \sqrt{\left(\frac{2LI_D}{C_{OX}\,W\mu_n}\right)_{M44}}}{1+(R_3/R_2)} \quad (11)$$

Where channel lengths of M3 and M4 are equal and their threshold voltages are close. Therefore, temperaturebehaviour of the Gate-Source voltage is only affected by the channel width of M33 and M44. In other words, M44 must be greater than M33 and should be WM33=2.38WM44.

It is obvious from (9) that IR1 has proportionate changing with temperature and bias the M3 and M4 as a current mirror with equal currents. These equal currents bias the M33 and M44 with diode connecting in strong inversion.

The (11) comprises two terms, the first one is V_1 which has inverse relation with temperature ($V_{tn33} > \sqrt{\left(\frac{2LI_D}{C_{OX}\,W\mu_n}\right)M_{33}}$), and the second term is V_2 which is proportional to temperature

($V_{tn44} < \sqrt{\left(\frac{2LI_D}{C_{OX} W\mu_n}\right)_{M_{44}}}$). Fig.3. demonstrates how the value of voltage level is reduced using R4 and R5. In this circuit, the output voltage is calculated 466.7mv according to (12).

$$v_{ref} = \frac{V_{ref}}{1+\frac{\left(R_2+\left[\left(\frac{1}{g_{m33}}\right)\|(ro_{m33})\right]\right)\|\left(R_3+\left[\left(\frac{1}{g_{m44}}\right)\|(ro_{m44})\right]\right)}{R_4+R_5}} \quad (12)$$

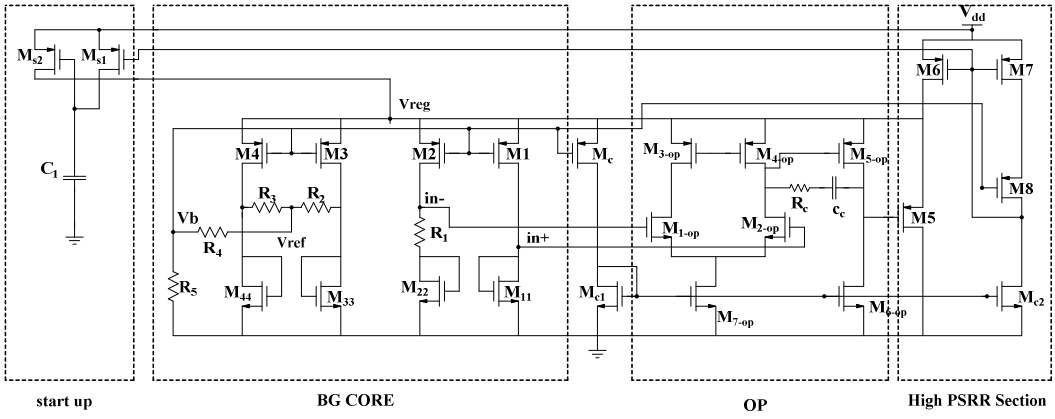

Fig. 3. Detailed schematic of proposed circuit

The complete proposed band gap voltage reference including the main core, regulated supply voltage VREG, operational amplifier, start-up circuit and a module used to improve PSRR is shown in fig.4. The aspect ratio of the various parts utilized in the proposed circuit and the designed amplifier are given in table 1 and table 2, respectively. The utilized operational amplifier is a two stage op-amp with a high DC gain which is shown in fig.4. This characteristic causes improvement in PSRR and reduction in error rate in the output voltage. In order to reduce the input offset in the op-amp, M1-op and M2-op NMOS transistors with large aspect ratios have been used. Simulation results for the two-stage amplifier are given in table 3.

Furthermore, nulling resistor technique is used for frequency compensation of this circuit in order to obtain appropriate phase margin and compensation network consisting of Cc and Rc. This operational amplifier is shown in fig.3. fig.4 shows the frequency response for the mentioned operational amplifier.

Table1. Transistors aspect ratios of Fig.3

$(\frac{W}{L})_{M1}$	$7.7\mu m/5\mu m \quad m=1$	$(\frac{W}{L})_{mS1}$	$1\mu m/15\mu m \quad m=1$	$(\frac{W}{L})_{m44}$	$8.4\mu m/5\mu m \quad m=1$
$(\frac{W}{L})_{M2}$	$7.7\mu m/5\mu m \quad m=1$	$(\frac{W}{L})_{mS2}$	$15\mu m/5\mu m \quad m=1$	C_1	952 f
$(\frac{W}{L})_{M3}$	$20\mu m/5\mu m \quad m=2$	$(\frac{W}{L})_{Mc}$	$5\mu m/5\mu m \quad m=1$	$R_1\left(\frac{L}{W}\right)$	143.73 µm/2.1µm rppo1rpo 22k

$(\frac{W}{L})_{M4}$	$20\mu m/5\mu m \quad m=2$	$(\frac{W}{L})_{Mc1}$	$7\mu m/10\mu m \quad m=1$	$R_2\left(\frac{L}{W}\right)$	130.66 µm/2.1µm rppo1rpo 20k
$(\frac{W}{L})_{M5}$	$10\mu m/5\mu m \quad m=1$	$(\frac{W}{L})_{Mc2}$	$7\mu m/10\mu m \quad m=1$	$R_3\left(\frac{L}{W}\right)$	130.66 µm/2.1µm rppo1rpo 20k
$(\frac{W}{L})_{M6}$	$35\mu m/5\mu m \quad m=5$	$(\frac{W}{L})_{M11}$	$1.44\mu m/5\mu m \quad m=1$	$R_4\left(\frac{L}{W}\right)$	157 µm/2.1µm rppo1rpo 24k
$(\frac{W}{L})_{m7}$	$5\mu m/5\mu m \quad m=1$	$(\frac{W}{L})_{M22}$	$2\mu m/5\mu m \quad m=1$	$R_5\left(\frac{L}{W}\right)$	464.48 µm/2.1µm rppo1rpo 71k
$(\frac{W}{L})_{M8}$	$5\mu m/5\mu m \quad m=1$	$(\frac{W}{L})_{M33}$	$20\mu m/5\mu m \quad m=1$		

Table2. Transistors aspect ratios of Op-Amp used in Fig.3

$(\frac{W}{L})_{M1-op}$	$10\mu m/5\mu m \; m=1$	$(\frac{W}{L})_{M4-op}$	15µm/5µm m = 1	$(\frac{W}{L})_{M7-op}$	18µm/5µm m = 2
$(\frac{W}{L})_{M2-op}$	$10\mu m/5\mu m \; m=1$	$(\frac{W}{L})_{M5-op}$	12µm/5µm m = 1	C_c	1 Pf
$(\frac{W}{L})_{M3-op}$	$15\mu m/5\mu m \; m=1$	$(\frac{W}{L})_{M6-op}$	11.9µm/5µm m = 1	R_c	50k

Table3. Op-Amp simulation results

Parameters	Simulation Results
DC Gain	64 dB
Unity Gain Bandwidth	6.4 MHZ
Phase Margin	59 degree
Input Offset	$39.7\mu V$
Current consumption	$10.638\mu A$

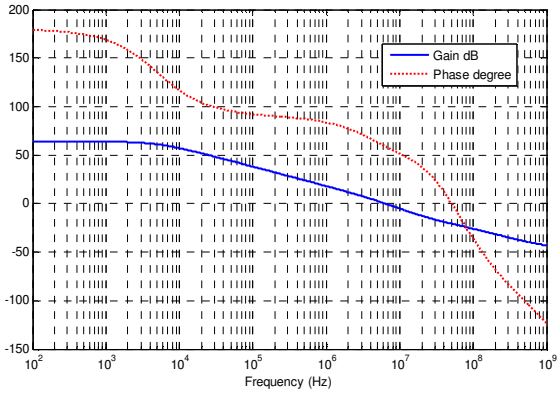

Fig. 4. Frequency response of simulated Op-Amp

2.1 Start-up Circuit

The startup circuit is shown in Fig.4.This circuit injects current into the core of Band Gap circuit. Ms1 transistor in startup circuit is combined with the high PSRR section in figure 4 In order to

reduce power dissipation. Ms1 and Ms2 startup transistors are biased with supply voltage and drain of Ms1 is connected to the ground by capacitor (C1). Ms2 drain injects a current into the core of the Band Gap circuit. Mc copies a fraction of current of the core circuit from M1-M4 current mirror and uses it to bias the OP-AMP accompanied by Mc1 and M7-op.MC2 mirror

transistor transfers Ib to M6 and M7 and the drain of MS1 startup transistor copies a partial current of M6 and M7 which causes increase in voltage across C1 to supply voltage value. Increase in voltage across the capacitor which is connected to MS2 gate makes MS1 and MS2 enter linear and cut-off regions, respectively. Finally proper current caused by by MS2 flows through the band gap voltage reference circuit. Gates voltages of MS1, MS2 and output voltage with versus startup circuit performance are shown in Fig.5. Settling time of the output voltage is 31µs. During settling time, startup circuit operation is independent from the core of the band gap circuit.

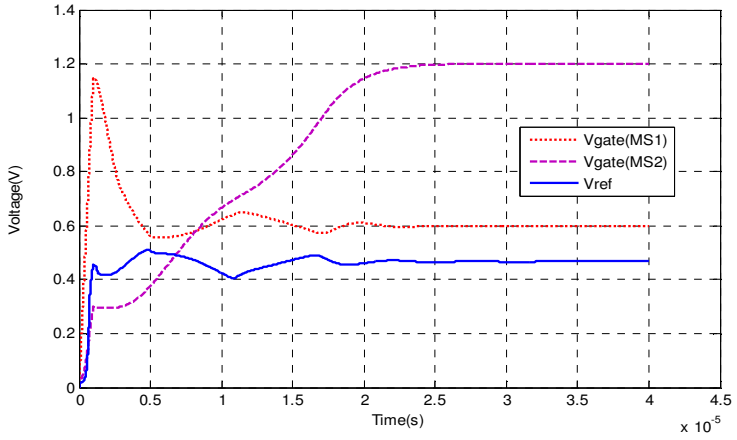

Figure 5. Output voltage and gates voltages of Ms1 and Ms2

2.2 High Power Supply Rejection Ratio

The PSRR in the proposed structure is enhanced using regulated voltage of Vreg. Mirror currents in M6 and M7 transistors provide regulated voltage Vreg as power supply for the core. The current source Ib which is shown in Fig.2 is independent from supply voltage and is a fraction of the current flowing through M1-M4. This structure separates the regulated voltage and supply voltage. This structure separates the regulated voltage from supply voltage. In comparison with the conventional band gap circuits, in this structure supply voltage required decrement is equal to the drain-source voltages of M6 and M7. In addition, M8 is biased in connection with M1-M4 in cascade configuration. The effects of supply voltage noise on regulated voltage Vreg is attenuated using following techniques.

1. Using Cascode current source configuration.
2. Utilizing a feedback loop. Feedback loop in Vreg node using a high gain op-amp amplifies the voltage difference between +in and –in nodes.

The loop gain in this structure is relatively high and is calculated from (13).

$$\text{PSRR} = \frac{V_{ref}}{V_X} \times \frac{V_X}{V_{REG}} \times \frac{V_{REG}}{\text{V}_{\text{ac}}} = \frac{\left(\text{V}_{\text{ref}}/\text{V}_{\text{ac}}\right)\text{open loop}}{1+\text{LG}} \quad (13)$$

Where Aop represents the operational amplifier gain, gm and ro are the transconductance and MOSFET output resistance, respectively. Since the size of M1 and M2 and the current flowing through them are equal, their transconductances are subsequently equal, gm1=gm2. 1/gm11 and 1/gm22 are small signal resistances of M11 and M12 as diode connected transistors. Large output resistances of M11 and M22 can be ignored in comparison with their small signal resistances.In addition, equivalent transconductance is g_{meq} which has been described in (14).

$$\text{R}_\text{L} = \left[\left(\left(\frac{1}{\text{g}_{\text{m33}}}\right) \| \left(\text{ro}_{\text{m33}}\right)\right) \| \left(\text{R}_2 + 2[\text{R}_4 + \text{R}_5]\right)\right] \| \left[\left(\left(\frac{1}{\text{g}_{\text{m44}}}\right) \| \left(\text{ro}_{\text{m44}}\right)\right) \| \left(\text{R}_3 + 2[\text{R}_4 + \text{R}_5]\right)\right] \quad (14)$$

PSRR for proposed circuit is presented in equation (15).

$$\text{g}_{\text{mx}} = \text{g}_{\text{m3}} + \text{g}_{\text{m4}} \quad (15)$$

Whew Vreg, Vref and Vac in (15) are supply voltage, output voltage and regulated voltage of proposed band gap reference, respectively.

$$\text{V}_{\text{ref}} = \text{V}_\text{x} \frac{2(\text{R}_4+\text{R}_5)}{2(\text{R}_4+\text{R}_5)+\text{R}} \quad (16)$$

2.3 Simulation Results

The proposed circuit is designed and simulated using TSMC 0.18µm technology with 1.2 V as supply voltage. Output voltage variations versus supply voltage are plotted in Fig.6 which is almost equal to the constant value of 466.7 mV for larger voltages.

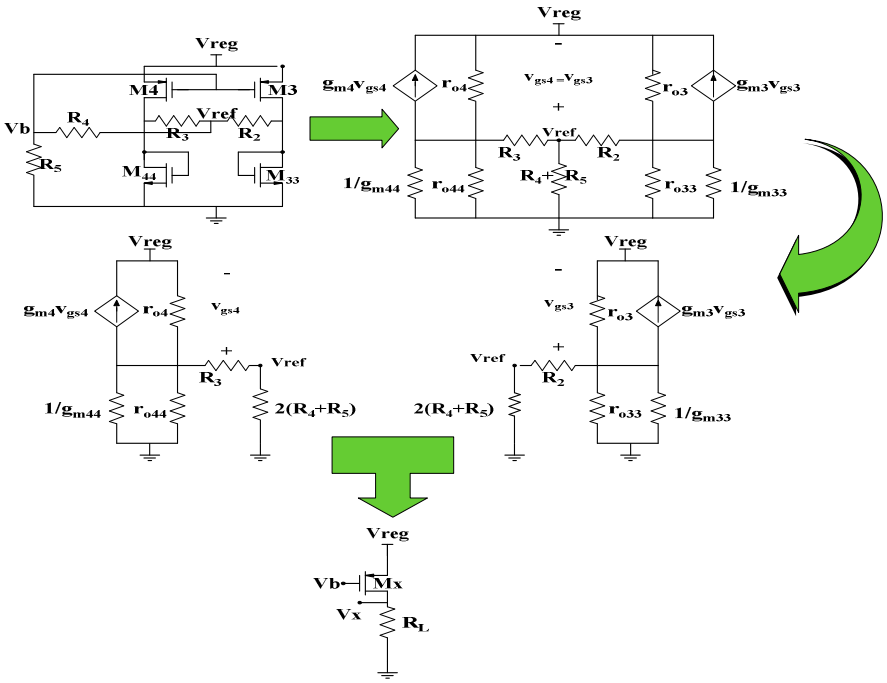

Figure 6. Output stage of Fig.2 circuit

Output voltage variations versus temperature ranging from -20C° to 100C° is shown in Fig.7. Maximum deviation of output voltage in this range is 3.5 mV. Output voltage level is the lowest at 45C. Temperature coefficient of the output voltage for the simulated circuit is 29.16, which guarantees a reasonable temperature performance. Variations in V1 and V2 are shown in Fig.8.

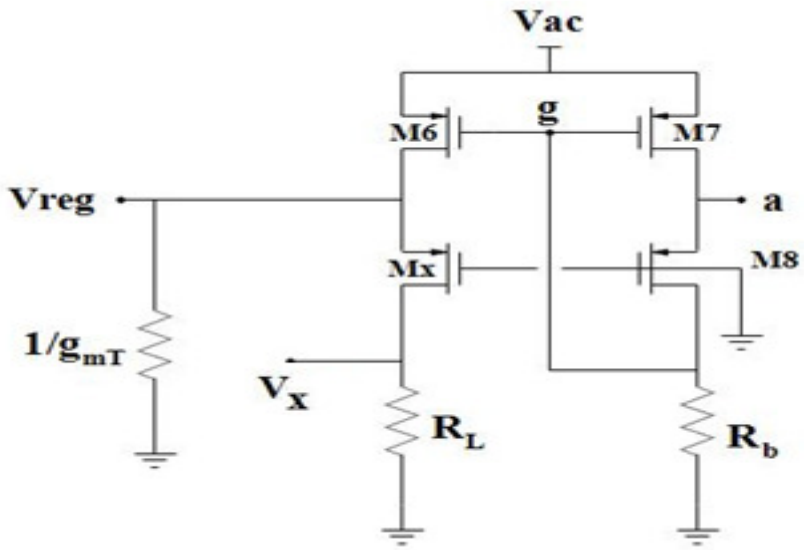

Fig 7. General part of high PSRR (Fig.3)

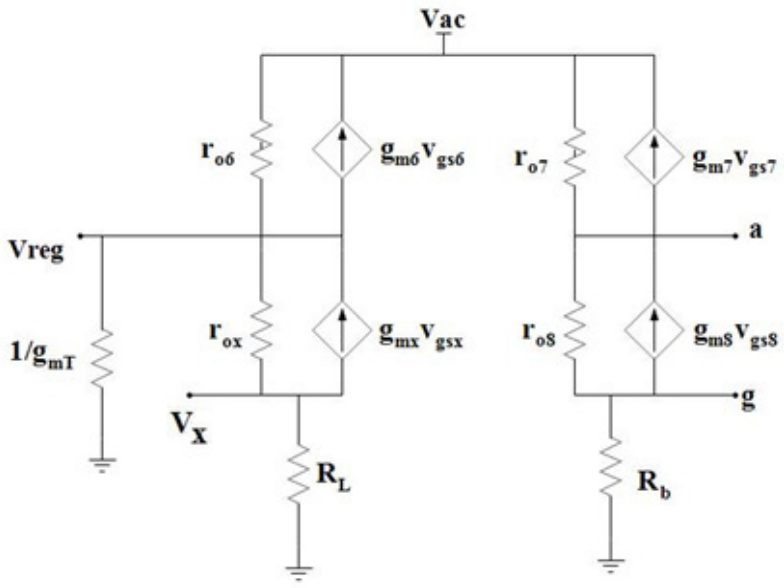

Figure 8. Small signal model of high PSRR part (Fig.7)

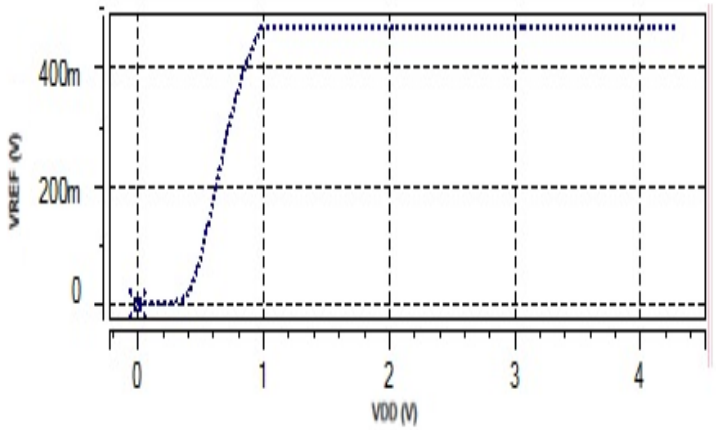

Fig 9. Output voltage versus power supply variation

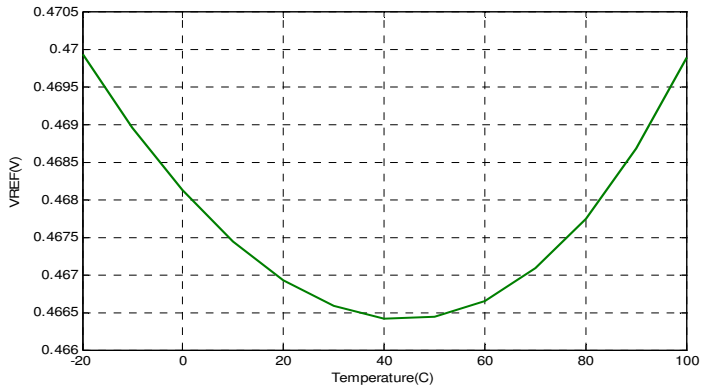

Fig 10. Output voltage versus temperature variation

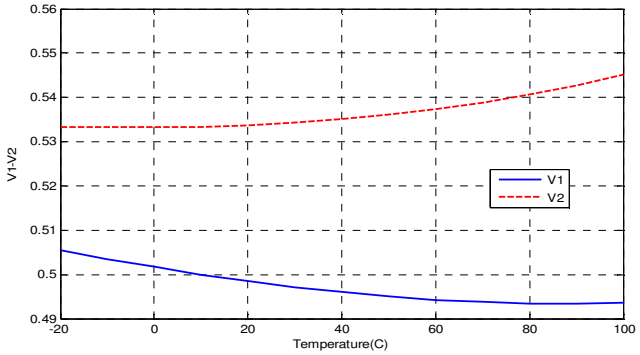

Fig 11. V1 and V2 versus temperature variation

In order to investigate the effect of mismatch in transistors on performance of the circuit, monte carlo method must be deployed in simulations. Each transistor which is defined is associated with a Gaussian Sigma function obtained from technology. Obtained results from simulating 100 sample band gap reference are given in table 4.

$$LG = A_{op}.\frac{g_{m5}}{g_{meq}}\left[\left(g_{m2} * (R_1 + \left(\frac{1}{g_{m22}} \parallel ro_{m22}\right)\right)\right) - \left(g_{m1} * (\frac{1}{g_{m11}} \parallel ro_{m11})\right)\right] \quad (17)$$

$$g_{meq} = g_{m1} + g_{m2} + g_{mx} + g_{m5} \quad (18)$$

$$g_{mT} = g_{m1} + g_{m2} + g_{m5} \quad (19)$$

Table 4. Simulation result of monte-carlo for proposed circuit

Sample Size	100
Maximum Value in Sample	0.49014
Minimum Value in Sample	0.44015
Average in data in Sample	0.46715

Median in data in Sample	0.46744

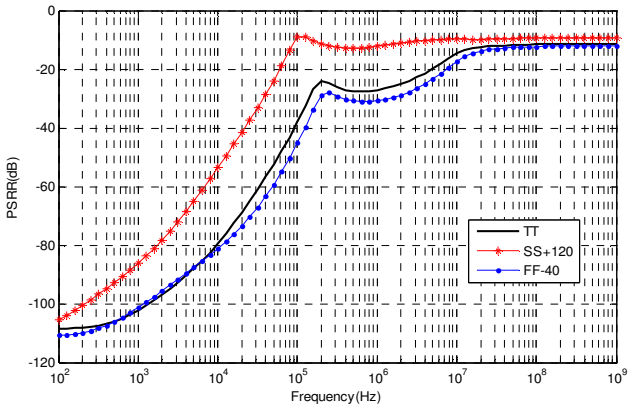

Fig 12. PSRR versus frequency for proposed circuit

Table.5 PSRR in corner cases

Process Corners	PSRR
TT	109 dB
TT+60	102 dB
FS	101 dB
SF	106 dB
SS+120	105 dB
FF-40	111 dB

According to equation (16), considering 1σ and 3σ, maximum output voltage deviation (from its nominated value) are ± 15.62 mV and 22.97 mV, respectively. The simulated histogram for the proposed circuit is shown in fig.9. PSRR of the proposed band gap voltage reference with 1.2v supply voltage for 5 process corners with various temperatures in DC frequency are given in table 5. These results have been obtained corresponding to process corner of 60C TT+60, fast process corner of -40C FF-40, slow process corner with 120C SS+120 and other process corners. In continue, PSRR of the circuit in a range of frequencies is shown in figure 10.

$$\left({V_x}/{V_{ac}}\right)\text{open loop} = \frac{V_x}{V_{REG}} \times \frac{V_{REG}}{V_{ac}} \tag{20}$$

$$\frac{V_x}{R_L} + \frac{V_x - V_{REG}}{ro_{mX}} + g_{mX}V_{gsX} = 0 \tag{21}$$

Table 6 shows the characteristics of the proposed band gap voltage reference in comparison with conventional works. "*" sign in table 6 denotes the results reported from fabrication process. All of the references in the table are simulated in CMOS technology. PSRR of the circuit is 109 dB at

low frequencies, 80 dB at 10 KHzand 27 dB at 1 MHz In a particular frequency range; the obtained PSRR is reasonably higher than the one in the conventional circuits. A scheme is exploited in order to reduce the sensitivity of the output voltage to supply voltage [7], and PSRR is 14 dB higher at lower frequencies. PSRR in the proposed circuit is 51 dB, 60 dB and 12 dB higher for lower frequencies, 10KHz frequency and 1 MHz frequency, respectively, in comparison with the voltage reference described in [10] which is relatively close to the designed circuit in power dissipation and output voltage. The band gap voltage reference provides higher PSRR and lower power dissipation in comparison with the voltage reference designed using MOSFETs in strong inversion region. The circuit's power dissipation is 42uW. Appropriate range for supply voltage in the design is 0.992v to 4.3v, which is comparatively reasonable. Moreover, the circuit suggests a relatively small temperature coefficient.

$$\frac{V_x}{V_{REG}} = g_{mx} * R_L \tag{22}$$

$$V_{reg} = V_{ac} * \frac{\frac{1}{g_{mT}+g_{mx}}}{\frac{1}{g_{mT}+g_{mx}}+ro_{m6}} - (g_{m6}V_{gs6}\frac{1}{g_{mT}+g_{mx}}) \tag{23}$$

$$\frac{V_g}{R_b} + \frac{V_g - V_a}{ro_{m8}} + g_{m8}V_{gs8} = 0 \tag{24}$$

$$\frac{V_g}{R_b} + \frac{V_g - V_a}{ro_{m8}} = g_{m8}V_a \tag{25}$$

$$V_g = V_a\left[\frac{R_b(1+g_{m8}ro_{m8})}{R_b+ro_{m8}}\right] \tag{26}$$

$$\frac{V_g - V_a}{ro_{m8}} + g_{m8}V_{gs8} = \frac{V_a - V_{ac}}{ro_{m7}} + g_{m7}V_{gs7} \tag{27}$$

$$\frac{V_g - V_a}{ro_{m8}} - g_{m8}(V_a) = \frac{V_a - V_{ac}}{ro_{m7}} + g_{m7}(V_g - V_{ac}) \tag{28}$$

$$V_a = \left[\frac{V_{ac}(ro_{m8}(1+g_{m7}ro_{m7}))}{(ro_7+ro_8\, g_{m8}ro_7-ro_8)-\left(\frac{R_b(1+g_{m8}ro_8)}{R_b+ro_8}(ro_7-ro_8\, g_{m7}ro_7)\right)}\right] \tag{29}$$

$$\%1\sigma = \frac{(Maximum-Average)}{Average} * 0.68 * 100 = 3.346\% \tag{30}$$

$$\%3\sigma = \frac{(Maximum-Average)}{Average} * 100 = 4.921\% \tag{31}$$

3. CONCLUSIONS

In this paper, a new method for designing an enhanced band gap reference using MOSFETs instead of BJTs was presented. MOSFETs in this design are in strong inversion region. Furthermore, a new technique for reducing sensitivity of the output voltage to supply voltage was introduced. Supply voltage selected is 1.2v. The proposed circuit have been simulated using TSMC 0.18 µm and HSPICE. According to simulation results, power dissipation, output voltage,

temperature coefficient and PSRR (in low frequencies) are 42 µW, 446.7 mV and 29.1 ppm/°C(-20°C to 100C°) and 109 dB, respectively.

Table.6. Comparison table

	[1]	[2]	[8]	[10]	[11]	Proposed SVR
Year Reported	2003	2012	2012	2011	2011	2014
CMOS Technology	0.25µm	0.18µm	0.18µm	0.5µm	0.5µm	0.18µm n − well cmos
V_{ref}	700 mV	1.204 V	343 mV	487.6 mV	228 mV	466.7 mV
Supply Range	1 to 2.5V	−−−−−−−	1.5 to 3.5V	1.2 to 3V	1 to 5V	0.992 to 4.3V
Power Dissipation	220µW	150 µW	117 µW	48 µW	28 µW	42 µW
Temperature Coefficient	0.3%	6.1 ppm/°c	3 ppm/°c	8.9 ppm/°c	34 ppm/°c	29.16 ppm/°c
Temp Range	0°c to 70°c	−20°c to 90°c	−40°c to 120°c	$-40°c\ to\ 110°c$	$-40°c\ to\ 120°c$	−20°c to 100°c
PSRR at DC	110 dB	84 dB	77 dB	58 dB	58 dB	109 dB
PSRR at 10KHZ	100 dB	44 dB	77 dB	20 dB	58 dB	80 dB
PSRR at 1MHZ	70 dB	20 dB	68 dB	15 dB	12 dB	27 dB

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