BULK-DRIVEN CURRENT CONVEYER BASED- CMOS ANALOG MULTIPLIER

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ABSTRACT

Bulk-driven technique has been verified to be a promising candidate in the area of low-voltage lowpower techniques. In this paper, current conveyer based-multiplier utilizing bulk-driven technique has been proposed. The proposed circuit was implemented based on CMOS technology to put a step forward in the field of low-voltage low-power applications. The circuit has been simulated at ±0.4 V supply voltage and total power dissipation 60.8 μW. The simulation results have been included to prove the theoretical consideration.

KEYWORDS

CMOS, Multiplier, Current Conveyer, Low-Power & Low Voltage

1. INTRODUCTION

Since a low voltage operating circuit becomes essential demand particularly in the case of portable devices, the current-mode technique is ideally suited for this purpose, more so than voltage-mode. Current-mode has many advantages such as, larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption [1]. Admittedly, bulk-driven (BD) principle has paved the way during recent years for low-voltage low-power applications [2-4]. In a conventional gate-driven (GD) MOSFET, the current is acquired when the gate-source voltage overcomes the threshold voltage. While in bulk-driven MOSFET, gate source voltage remains constant and the input signal is applied at the bulk terminal. Functionally seen, a bulk driven MOSFET is equivalent to the depletion type device JFET. Since BD is a depletion-type device, it can work under negative, zero, or even slightly positive biasing conditions [5], [6].

The bulk-driven technique has a few drawbacks, the most important of which is that the bulk transconductance g_{mb} is (3 to 4) times smaller than the gate transconductance g_m. Accordingly, the DC gain value and the bandwidth are relatively low compared to the gate-driven one. But it should be taken into account that, for example, active filters with low cutoff frequencies (in the range of few hertz up to few kHz) are needed in the field of medical electronics applications, due to the relatively slow electrical activity of the human body.

DOI : 10.14810/elelij.2015.4406

Current conveyor second generation CCII is active element exhibiting higher linearity, wider dynamic range and better high frequency performance compared to their voltage mode counterparts [7]. In this paper we present a multiplier based on bulk-driven current conveyor second generation CCII. The most important difference between this type of multiplier and [11],[12] and [18] is the ability of low voltage low power operation.

Our paper is organized as follows, in section 2 a brief description about BD MOST is shown, while in section 3 an implementation of CCII based on BD is illustrated. In section IV multiplier based on CCII and simulated results of the proposed circuit are described. At the end a conclusion is drawn.

2. BULK-DRIVEN CURRENT CONVEYER

From the discussions in the aforementioned section, it was discussed that bulk-driven technique has a few drawbacks. This section briefly discusses this issue. The transconductance of BD MOSFET is reduced compared with GD one.

$$g_{mb} = \frac{C_{bc}}{C_{gs}}.g_m = \eta g_m \tag{1}$$

Where C_{bc} is a bulk channel capacitance, C_{gs} is the gate source capacitance and η is in range of (0.2 to 0.4). The bandwidth of BD MOSFET is reduced compared with GD one.

$$f_{Tb} \approx \frac{g_{mb}}{2\pi\left(C_{bs}+C_{bsub}\right)} = \frac{\eta}{3.8}.f_T \tag{2}$$

Where, C_{bs} is a bulk source capacitance, C_{bsub} is the bulk substrate capacitance. As shown, the transconductance of a bulk-driven MOSFET is substantially smaller than a conventional gate driven MOSFET. This results in lower gain and bandwidth, but better linearity and less power supply requirements.

Fig. 1 illustrates the circuit schematic of a ±0.4V BDFC- class AB CCII. The proposed CCII consists of differential pair (M1, M2); the input signal is applied to the bulk terminal of the input transistors M1-M2, while the gate terminals of these transistors are connected to *VDD*, so as to provide an appropriate value for their gate-to-source voltage. The signal currents of the differential output are folded through transistors M9, M10 and converted to single ended signals with cascoded current mirror M11-M13. The second stage of OTA is created by transistors M14-M17. The X terminal current is then mirrored to the Z terminal by the action of cascoded current mirrors by transistors M18-M21; it is evident that both *IX* and *IZ* flow simultaneously towards or away from the CCII. Transistors M3-M8 and Ibias form the necessary voltage and current biases for the first stage of folded cascode structure. Capacitor Cc forms the compensation network.

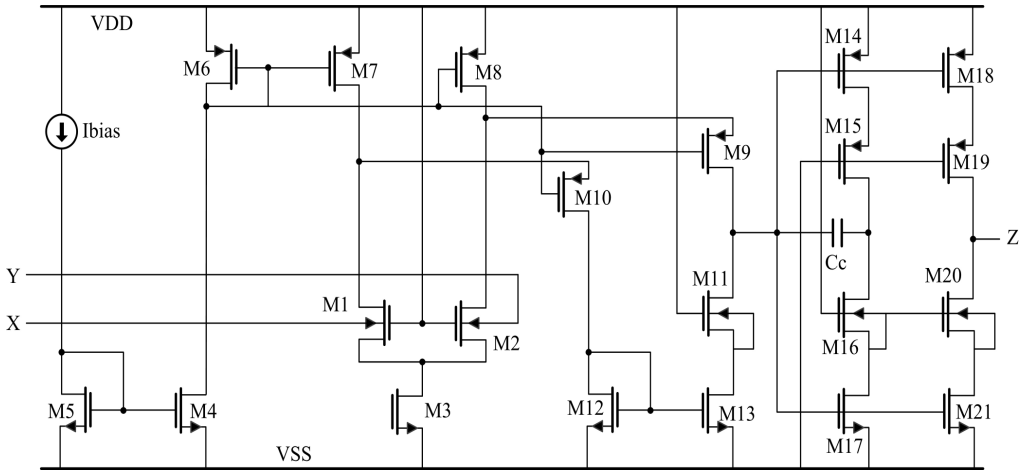

Figure 1. Bulk-Driven Second Generation Current Conveyer

Table 1. MOSFET Sizing of BDCCII

MOSFET's	Width	Length
M1,M2	60µm	0.5µm
M3,M18	11µm	3µm
M4,M6,M7,M8,M9,M10,M12,M13	10 µm	3 µm
M5	4 µm	3 µm
M11	10 µm	2 µm
M14	11 µm	3 µm
M15,M19	11 µm	1 µm
M16,M20	4 µm	10 µm
M17,M21	52 µm	2 µm

3. CMOS Multiplier based on CCII

In this section, different parts of analog multiplier circuit based on current conveyors will be described and analysed. The proposed circuit is shown in figure 2. In this figure, V_{in1} and V_{in2} voltages are input signals that their product will be appeared in the output. Also, in this figure, three stages of main multiplier circuit are shown that from left to right, there are input linear (Triode) transistors, current conveyors and current subtractor. It is essential to mention that in the second stage, two same current conveyors are used.

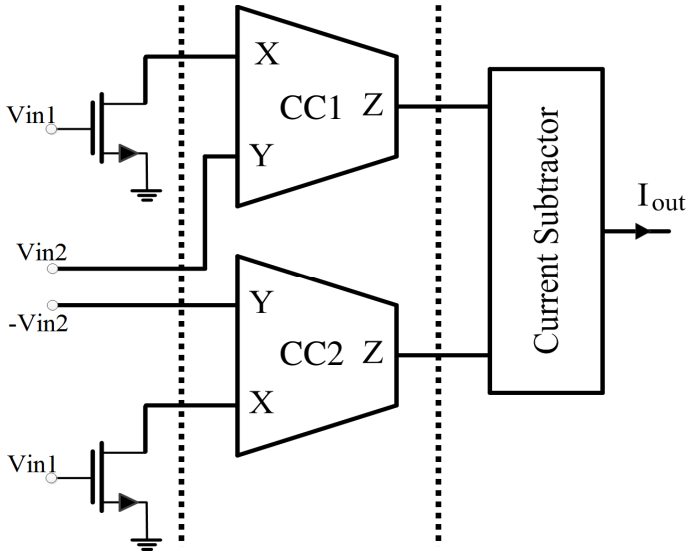

Fig2: Proposed Analog Multiplier

3.1 Input linear transistors

First stage of proposed multiplier is consisting of two N-Channel MOSFETs which are biased in linear region. Drains of these two transistors are connected to the X terminal of each of the two current conveyors in the second stage and one of the input signals accompanying DC bias voltage is applied to their gates. Applied DC bias voltage to the gate of these two transistors is chosen according to the DC voltage of X node in current conveyor and also according to enrich the (3) relation, so these transistors will be biased in linear region.

$$V_{DS} < V_{GS} - V_{th} \tag{3}$$

If these two transistors are biased in linear region, their current amount will be obtained from (4).

$$I_{DS} = \mu_n c_{ox} \frac{W}{L}\left((V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \tag{4}$$

From small signal point of view, the small signal current of these two transistor which is equal to the current of current conveyors is shown in (5) and (6).

$$i_{ds} = \mu_n c_{ox} \frac{W}{L}\left(v_{in1} v_{ds} - v_{th} v_{ds} \right) - \mu_n c_{ox} \frac{W}{L}\left(\frac{1}{2} v_{ds}^2 \right) \tag{5}$$

$$i_{ds} = \mu_n c_{ox} \frac{W}{L}\left(v_{in1} v_X - v_{th} v_X \right) - \mu_n c_{ox} \frac{W}{L}\left(\frac{1}{2} v_X^2 \right) \tag{6}$$

In (6), V_X is the input voltage of terminal X of current conveyor and its amount is equal to V_{DS} in linear transistors. Equation 4-4 has two parts that one is only consist of V_X and the other one is only consist of V^2_X. In the first part, $V_{in1}V_X$ term presents the product of two signals in the input of current conveyors X terminal and linear transistor gates. This product can be considered as a base for producing the multiplication of the two inputs.

The second part of small signal current of these two transistor, is an extra factor that should be eliminated. The elimination of this part is done in current conveyors and current sabtractor.

3.2 Current Subtractor

The last stage of proposed multiplier is a current subtractor. This circuit shown in figure3, subtract output current of CCII [17]. Size of MOSFET's in subtractor circuit reported in Table 2.

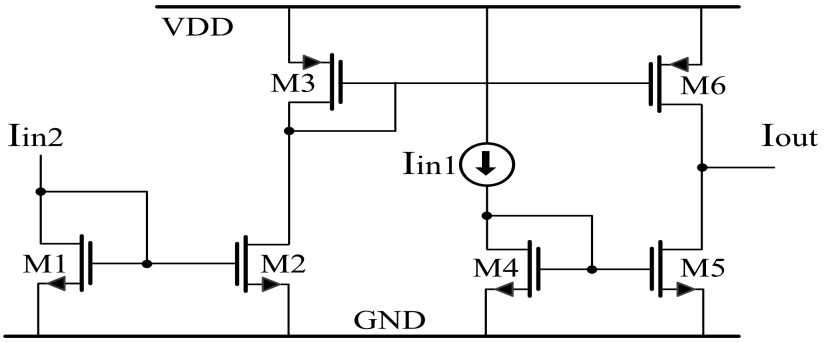

Figure 3. Current Subtractor

Table 2. MOSFET Sizing of Subtractor

MOSFETS	Width	Length
M1,M3,M5,M6	0.44µ	0.18µ
M2	0.39µ	0.18µ
M4	0.43µ	0.18µ

4. Simulation Result

To validate the results found in the previous sections, we simulated with HSPICE the circuit shown in Figure. 2 where the BDCCII block detailed in Fig. 1. The circuit was simulated using the TSMC 0.18µm CMOS process. Supply voltage was ± 0.4V. Fig. 4 shows the frequency response for X terminal of BDCCII. The total power consumption of the multiplier is less than 60.8µW. Figure.5 illustrates the time response of multiplier. Also Table.3 shows comparison between proposed circuit with other existing works.

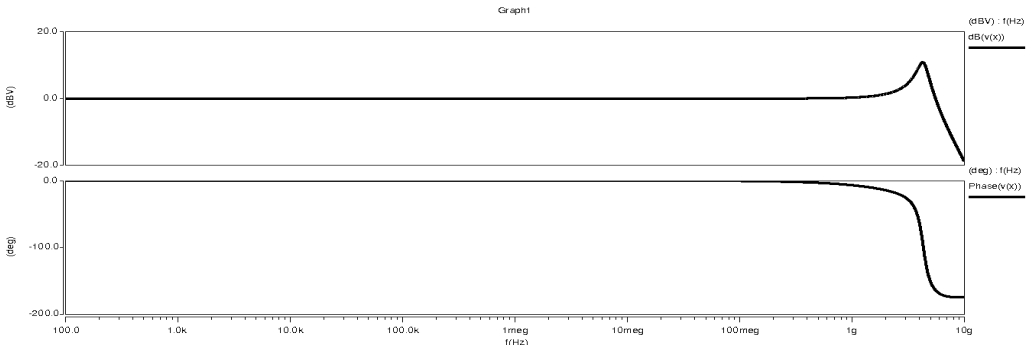

Figure4. Frequency response of X terminal

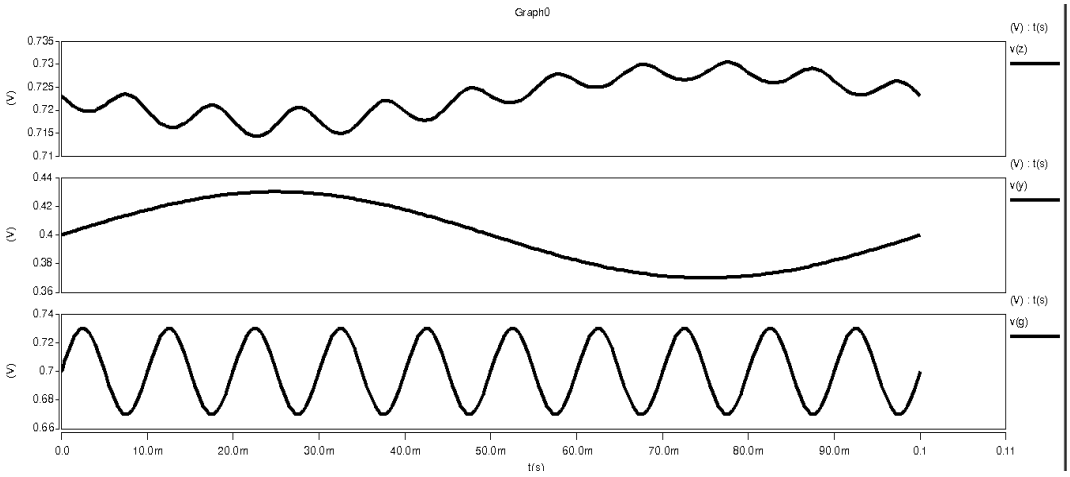

Figure 5. Input and output signals in time domain

Table 3. Comparison with the existing analog multiplier

	Supply Voltage (V)	Power Consumption (µW)	THD (%) (1MHz)	Non linearity (%)	-3dB Bandwidth (MHz)	Technology (µM)
[13]	2	55	1	5	0.2	0.35
[14]	5	930	0.65	1.2	22.1	2
[15]	± 1.5	460	3.7	1.25	19.3	0.5
[16]	3.3	240	0.76	1.15	44.9	0.35
This work	± 0.4	60.8	4	5	200	0.18

3. CONCLUSIONS

The design of a Low-Power Low-Voltage, multiplier based on BD CCII in a standard CMOS process is reported in this paper. Simulated circuit characteristics show that the proposed circuit exhibits a very good performance. The proposed circuit was simulated using the TSMC 0.18µm CMOS process. Supply voltage was ± 0.4V. The total power consumption of the multiplier is less than 60.8µW.

Acknowledgments:

This work was supported by the Iran Analog Research Group (IARG) under grant number IARG-941. The authors are grateful for the assistance of Microelectronics Laboratory members for consultation support and specially Mr. Gholamreza Hadidi (Shagholam) and Sadegh Biabanifard for their contribution to design the proposed multiplier.

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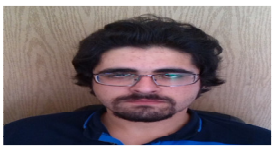

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