LOW POWER MULTIPLIER DESIGN WITH IMPROVED COLUMN BYPASSING SCHEME

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ABSTRACT

Power, speed and area are prime design constraints for portable electronics devices and signal processing applications. Multiplier plays an important role in DSP applications. In this paper, a low power and high speed multiplier with improved column bypassing scheme is presented. Primary power reduction is obtained by disabling the supply voltage of non-functional blocks when the operands of the multiplicands are zero. Power reduction is achieved by both architecture and circuit level modifications. The proposed multiplier consists of new adder architecture which is also responsible for reducing the power consumption and propagation delay. Simulation results are obtained with UMC 90nm and 0.9 V CMOS technology with cadence spectre simulation tool. The proposed multiplier has been compared with popular multipliers and performance parameters in terms of power dissipation, speed and area occupation are found better. The proposed multiplier is definitely a better choice for low frequency (≤ 50 MHz) applications. The results are obtained for randomly generated input test patterns having uniform distribution probability and more power can be saved if operands have more 0's than 1's.

KEYWORDS

low power, delay, area overhead, switching transitions, adder, multiplier.

1.INTRODUCTION

To develop low power, high speed and area efficient portable electronic design is a very challenging problem for the hardware designers in the current scenario [1]. Mobile phones, smart cards, assistive listening technology such as hearing aids and PDAs are the example of portable consumer electronic products [2, 3]. The main concerns of these products are not only to extend the operating hours of the battery residing in it but also great computational capacity. Low power design can be develop at system level, technology level, architecture level and circuit level. A larger amount of power can be saved if low power design is achieved at system level. A significant amount of power consumption can be reduced at architecture level but at the cost of delay penalty and area overhead. At architecture and system level, parallelism and pipelining are two main techniques used to reduce power and propagation delay [4]. At technology level, power consumption is going to scale down at the same time as the technology is shrinking day by day. Thus, power saving can be achieved by the improvement in fabrication process such as small

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feature size, very low voltages, interconnects and insulator with low dielectric constants. At circuit level voltage scaling, threshold voltage, Transistor sizing, network restructuring power down strategies and logic style are used to achieve low power [5]. In addition to this, this technique also contributes in the reduction of propagation delay and area occupancy as well.

Digital signal processing (DSP) is a important unit in electronic devices. Digital Signal Processors (DSPs) are used to perform the common operations such as video processing, filtering and fast fourier transform (FFT). Such modules perform extensive sequence of multiply and accumulate computations. Multiplication is most fundamental operation in digital computer systems and digital signal processors [6-9]. A large number of transistors with high switching transitions is used to perform variety of multiplication operations. Multiplier consumes 30% power and also occupies 46% chip area in 64 point radix-4 pipelined FFT processor. Therefore, multiplier is most critical, power hungry arithmetic unit that requires more area and computational time [10-15]. Various techniques are applier externally and internally in the past, to achieve energy efficient multiplier designs. External techniques are related to the input data characteristics, whereas an internal technique deals with the system, technology, architecture and circuit level [6]. In literature, different tree based multipliers (Wallace and Dadda) and array based multipliers are discussed extensively [16-19]. Array based multipliers consumes low power as compared to Wallace tree multipliers. In tree based multiplier, additional hardware is require to improve the performance, but at the cost of increased layout and parasitic. On the other side, array multiplier has smaller and regular layout. Therefore, array multiplier is a better choice due to its lower power consumption, smaller layout and relatively good performance [20-23]. Adder is a fundamental unit of the multiplier, thus it has significant impact on the overall performance of the system in terms of power dissipation, delay and area occupancy.

In this paper, array multiplier is proposed to achieve low power and high speed multiplication operation with lesser hardware cost. This multiplier adopts improved column bypassing scheme and new adder architecture for better overall performance. The proposed adder architecture is optimized with lesser hardware as small area leads to less switching transitions.

The rest of the paper is organized as follows. Section 2 presents a short introduction to the sources of power dissipation. Section 3 reviews the various multipliers. Section 4 describes the proposed multiplier. Results and analysis of the entire work are presented in section 5. Finally, Section 6 concludes the paper.

2.POWER DISSIPATION

The sources of power consumption in digital CMOS circuits are static power dissipation and dynamic power [24-26]. Eq. (1) shows power consumption of digital CMOS circuits [27].

$$P_{total} = \alpha f C_L V_{DD}^2 + I_{SC} V_{DD} + I_{leakage} V_{DD} \quad (1)$$

Where α is switching transition of a clock cycle, C_L is the output capacitance, V_{DD} is the supply voltage and f is the switching frequency which is fixed in many DSP and dedicated applications, *Isc* is the short circuit current, and $I_{leakage}$ is the leakage current [28]. In the submicron technology, leakage current is a significant contributor of power consumption. Circuit and

technology level techniques used dual V_t partitioning, multi-threshold CMOS and power gating approach to reduce the leakage power. Some leakage reduction methods have been presented in [29, 30]. Power gating approach can reduce both the components of power dissipation up to a good extent [31-33]. In this paper, power gating approach is consider for the power reduction of proposed multiplier. This technique uses sleep transistors to shut down the supply of the selective logic blocks which are not functional during bypassing operation. PMOS transistor acts as a header switch to connect the supply voltage V_{DD} to logic block and NMOS acts as a footer switch to connect the ground to the logic block [34] as shown in figure 1. The proposed multiplier utilizes power gating approach and used PMOS header switch in place of tri state buffer which are used by the previously discussed multipliers.

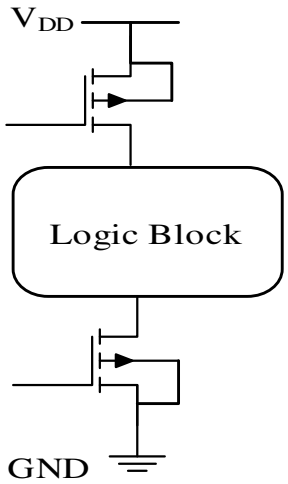


Figure 1. Power gating technique

In an active circuit, dynamic power dissipation is the major source of power dissipation where leakage power is less. Dynamic power can be lowered by reducing the switching transitions of the design without affecting its functionality. Most of the power reduction techniques apply on the multiplier target optimization of parameters involved in equation (1), Logic style and optimized architectures are also used to reduce the power consumption. In case of multiplier, dynamic power can be reduced quarterly by reducing the supply voltage but makes the module sluggish [35]. This further reduces the throughput since the delay T_d is inversely proportional to the supply voltage as shown in eq. (2)

$$T_d = \frac{C_{load} V_{sup\,ply}}{\left(V_{sup\,ply} - V_{th}\right)^2} \tag{2}$$

where V_{th} is threshold voltage of the transistor, C_{load} is the load capacitance. In the short channel device, the value of $V_{supply} - V_{th}$ is 1.3 in the above equation. It varies according to the technology and assumed to be fixed. In this paper, we focus on reducing both dynamic power dissipation and static power dissipation with architecture level and circuit level modifications.

3.REVIEW ON MULTIPLIER ARCHITECTURES

Multiplication is the basic operation performed by many common DSP functional unit such as FIR filters and FFT modules. Reduction in the power consumption of the multiplier can reduce a significant portion of the power in the overall digital system [36]. The multiplication of n bit wide numbers A and B is defined as follows [37].

$$P = A \times B = \sum_{i=0}^{i-1} \sum_{j=0}^{j-1} \left(\left(A_i B_j \right) 2^{(i+j)} \right) \tag{3}$$

Where P represents the products, A_i is i^{th} bit of multiplicand and B_j is j^{th} bit of multiplier. A 4(x)4 basic multiplication is shown in figure 2.

			A =	a_3	a_2	a_1	a_0
		(×)	B=	b_3	b_2	b_1	b_0
				a_3b_0	a_2b_0	a_1b_0	a_0b_0
			a_3b_1	a_2b_1	a_1b_1	a_0b_1	
		a_3b_2	a_2b_2	a_1b_2	a_0b_2		
	a_3b_3	a_2b_3	a_1b_3	a_0b_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Figure 2. A 4(x) 4 basic multiplication

3.1.Conventional Array Multiplier

Array multiplier is a better choice in DSP applications due to its smaller layout and high throughput. It is based on standard add and shift operations. Its structure is organized by several stages of AND gates and full adder cells. It may consist of either ripple carry adders (RCAs) and carry save adders (CSAs)[38]. For N(x)N multiplication RCAs based multiplier needs 3N adders and takes 2N+1 adders delay in the worst case. However CSAs based multiplier needs 3N adders to perform multiplication but takes N + 2 adders delay in the worst case. In CSA based multiplier,

carry has to be propagate from $(j-1)^{th}$ row to j^{th} row and then $(j+1)^{th}$ row. The CSA based parallel array multiplier is also known as braun Multiplier [39] as shown in figure 3.

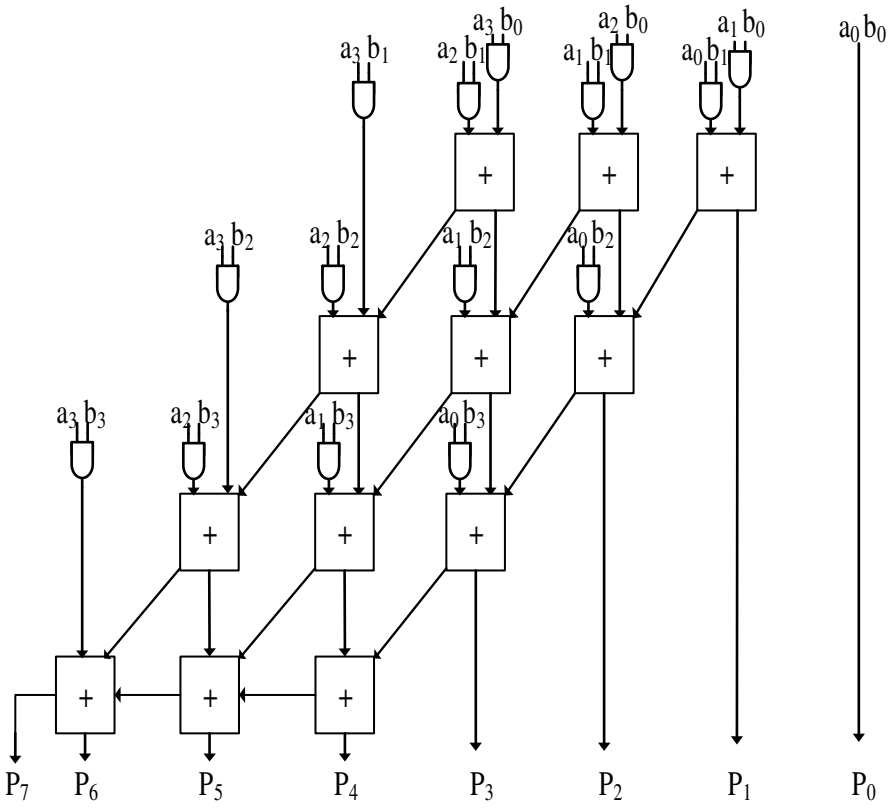


Figure 3. Braun Multiplier

The limitations of the braun multiplier is its logical architecture that leads to more power consumption and hardware cost. Power reduction can be achieved through architectural modification via row bypassing, column bypassing, row and column bypassing and circuit level modification. Based on the concept of improved column bypassing with new adder architecture, a low power and high speed multiplier is proposed with lesser hardware cost.

3.2.Column Bypassing Multiplier

Column bypassing multiplier eliminates the extra correcting circuit to skip the full adder cell and also consumes lesser power than braun multiplier at higher frequency of operation. This multiplier consists of rows of carry save adders. The major focus of this multiplier is to reduce the switching transitions required to perform the computations. The adder cell is shown in figure 4.

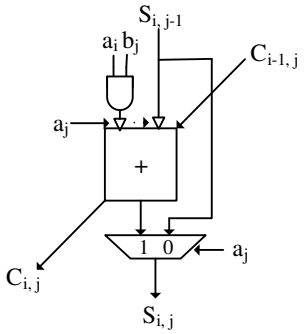


Figure 4. Modified carry save full adder

Tri-state buffers at the input of the adder cells are inserted for reducing the switching transitions if these cells are bypassed. Whereas, Multiplexer is inserted to select the sum output under no bypassing condition or when the bypassing is used as shown in figure 5. The addition operation in $(i-1)^{th}$ column can be bypassed to $(i)^{th}$ if the corresponding bit in the multiplicand is zero. This operation is performed by disabling adder with buffer under the control of multiplier bit a_i [40, 41].

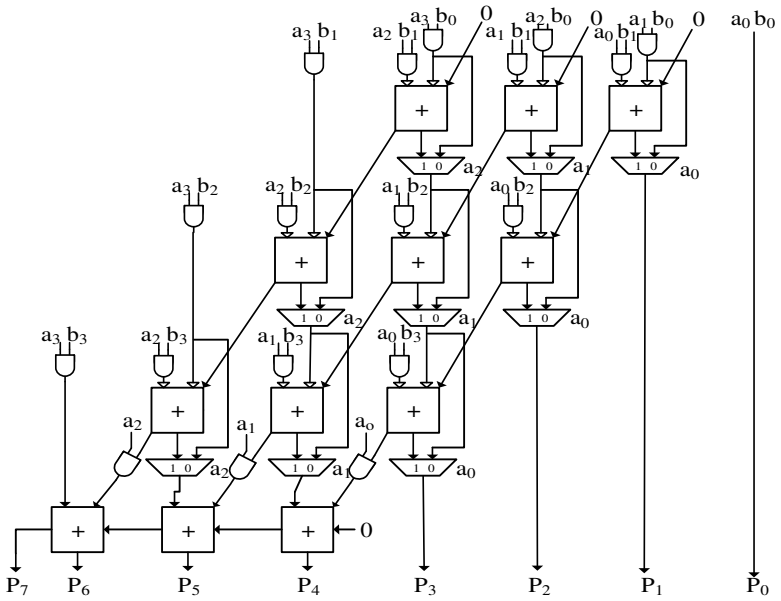


Figure 5. A 4(×)4 column bypassing multiplier

The main limitations of this multiplier are its extra hardware cost and power consumption because of buffers, full adder cells and additional AND gates inserted in the last row of adder cells. While simulating, it was observed that this multiplier also dissipate large amount of power than conventional array multiplier due to the buffers if operating at lower frequencies.

3.3.Row Bypassing Multiplier

Row bypassing multiplier consumes lesser power than braun multiplier at higher frequency of operation. It consists of the rows of the ripple carry based full adder cells. The adder cell is shown in figure 5.

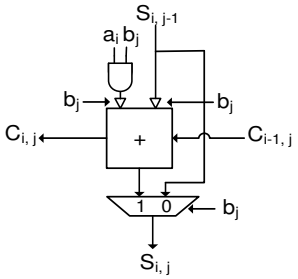


Figure 6. Modified ripple carry full adder

Tri-state buffers at the input of the adder cells are inserted for reducing the switching transitions, if these cells are bypassed. Whereas, multiplexer is inserted to select the sum output under no bypassing condition or when the bypassing is used as shown in figure 7. The $(j-1)^{th}$ row of adders are bypassed to $(j)^{th}$ row if the corresponding bit in the multiplier is zero. This operation is performed by disabling the adder with tri state buffer under the control of multiplier bit b_j. Buffers and multiplexers are designed with transmission gates [12].

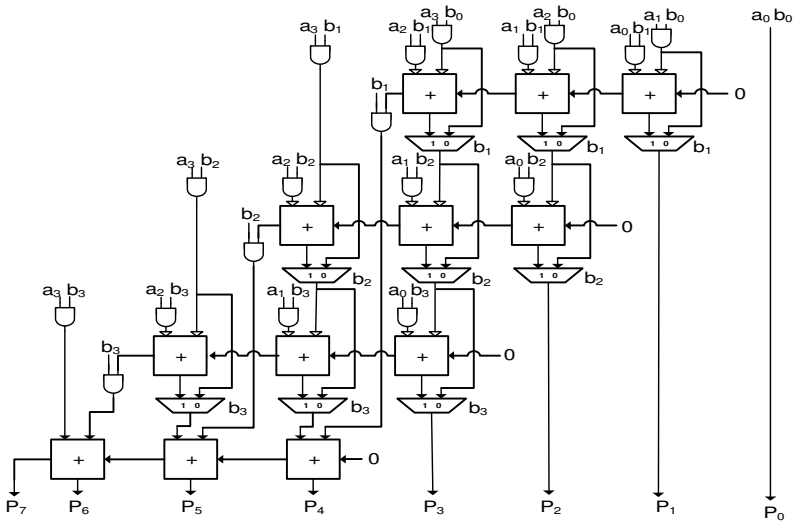


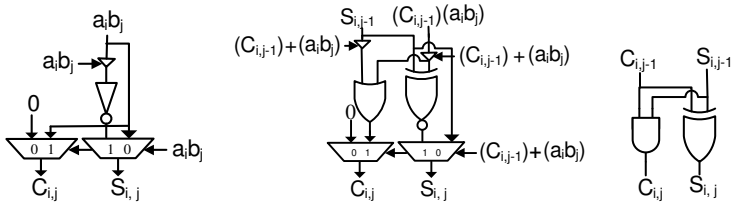
Figure 7. A 4(x)4 row bypassing multiplier

The limitation of this approach is that it consumes more power and also has extra hardware due to the use of buffers and full adder cells. While simulating, it was also observed that this multiplier

also dissipate larger amount of power than the conventional array multiplier due to the buffers if operating at lower frequencies.

3.4.Row and Column Bypassing Multiplier

This multiplier consumes lesser amount of power and lesser hardware than the previously discussed multipliers. The $(j-1)^{th}$ rows of the multiplier is bypassed under the control of AND gate (a_ib_j). When the output of gate (a_ib_j) is 1, the addition operation is performed by an inverter and the carry output will be equal to the input of the inverter as shown in figure 8(a). If (a_ib_j) is 0, the inverter is disabled with buffer and its input is bypassed to the sum output. Carry out will be zero because both remaining operand and carry-in is zero. This operation is applicable in the first row of the CSA based adder cell as the C_{in} is always zero.



(a) A+1 adder (b) A+B+1 half adder (c) A+B half adder

Figure 8. Different adders in multiplier design

In the preceding rows, full adder cell is replaced with half adder in the form of A+B+1 and A+B as shown in figure 8(b) and figure 8(c) respectively. The additional hardware used with half adder cell include OR gate, AND gate, two-tri-state buffers at the input and two 2:1 multiplexers at the output, to select the sum and carry outputs as shown in figure 9.

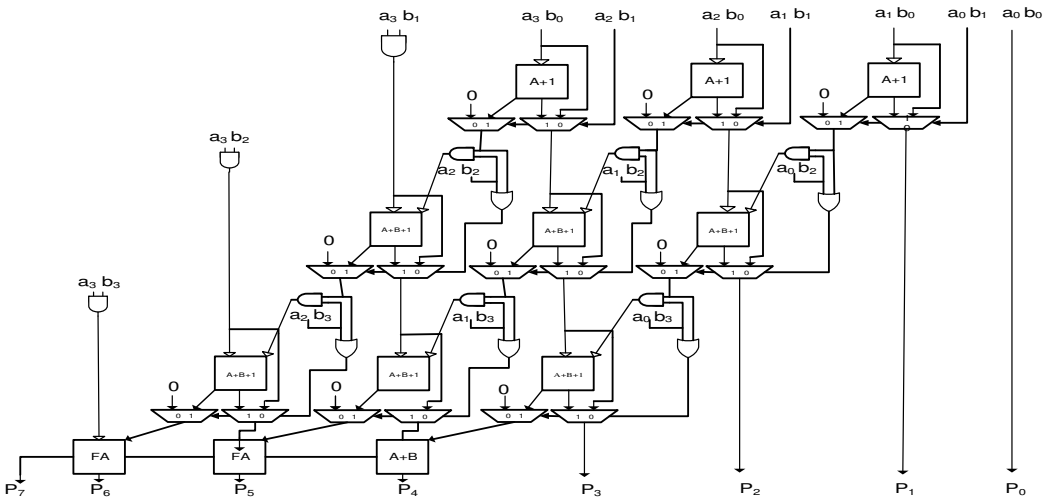


Figure 9. A 4(x)4 row and column bypassing multiplier

The $(j)^{th}$ rows of this multiplier is bypassed if the OR operation of previous carry-in ($C_{i,j-1}$) and operand (a_ib_j) is 0. When the output of OR gate is 1 then the addition operation is performed by half adder cell A+B+1 [42]. The main limitation of this multiplier is that it does not use bypassing approach and therefore consumes more power. In addition, this system is more complex and consumes larger amount of power at low frequencies due to the presence of no. of buffers.

4.PROPOSED MULTIPLIER

Array multiplier consists of rows of adder cells. The sum and carry signals generated from the previous rows are fed into the next rows. Evidently, adders are the major power and area consuming unit of the multiplier. The power consumption of a multiplier can be lowered by reducing the switching transitions and hardware cost of the adder cells.

Switching transitions at the adder cells of the proposed multiplier can be lowered using new improved column bypassing scheme (ICBS) achieved using power gating approach. The proposed multiplier selects the ICBS only if the multiplicand a_i is zero as shown in figure 11. Power gating saves more power by temporarily disabling the supply voltage (V_{DD}) to the selective blocks which are not functional during that period. Therefore, this approach leads to lesser power consumption and area than that of the buffers used by the previous designs. Besides, the performance of buffers is very poor at low frequencies. Hence buffers may not be good choice for low power, low frequency applications.

The occurrence probability of zero in a multiplier can be described by the following equation.

$$\sum_{i=1}^{n} prob(D_i)\times\left[\frac{i}{n}\times 50\% + \frac{n-1}{n}\right] + \sum_{i=-1}^{-n} prob(D_i)\times\left[\left|\frac{i}{n}\right|\times 50\% + \left|\frac{n-1}{n}\right|\right] \quad (4)$$

Where n is the number of bit in the multiplicand A and multiplier B, D_i is the effective data and prob is the probability of specified effective data. Based on the equation (4), the probability of zero in actual multiplier implementation such as adaptive differential pulse code, G723.1 speech code and wavelet based image coder is over 65%. This is more than uniform distribution probability [10]. This proves that bypassing used in multiplier is much better scheme for power saving. Therefore, the ICBS has been used to design the proposed multiplier. It has been tested that the proposed to be the best for low frequency applications (≤ 50 MHz) such as assistive listening technology. This multiplier also performs better for high frequency applications (≤ 333.3 MHz) than the designs available in the literature.

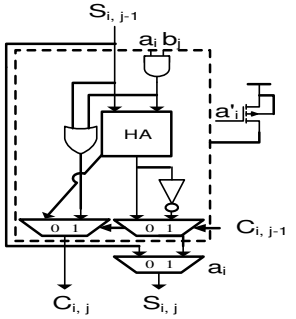


Figure 10. Proposed adder cell

Secondly, the new adder architecture reduces the power consumption when bypassing operation is not used. The addition operation in proposed multiplier is performed by new adder cells if a_i is 1 otherwise ICBS is selected by shutting down the proposed adder unit with power gating approach. The new adder architecture as shown in figure 10 has been designed using fewer hardware components. This adder has lesser area, propagation delay and power requirement than the previously discussed multipliers. If carry-in is 0, the addition operation is performed by the half adder and sum and carry outputs are selected by multiplexer. The inverted output of half adder cell and or operation of half adder inputs are selected by multiplexer as sum and carry output, if carry-in is 1. Hence, the functionality of full adder cell is obtained using reduced number of transistor in the proposed adder cell.

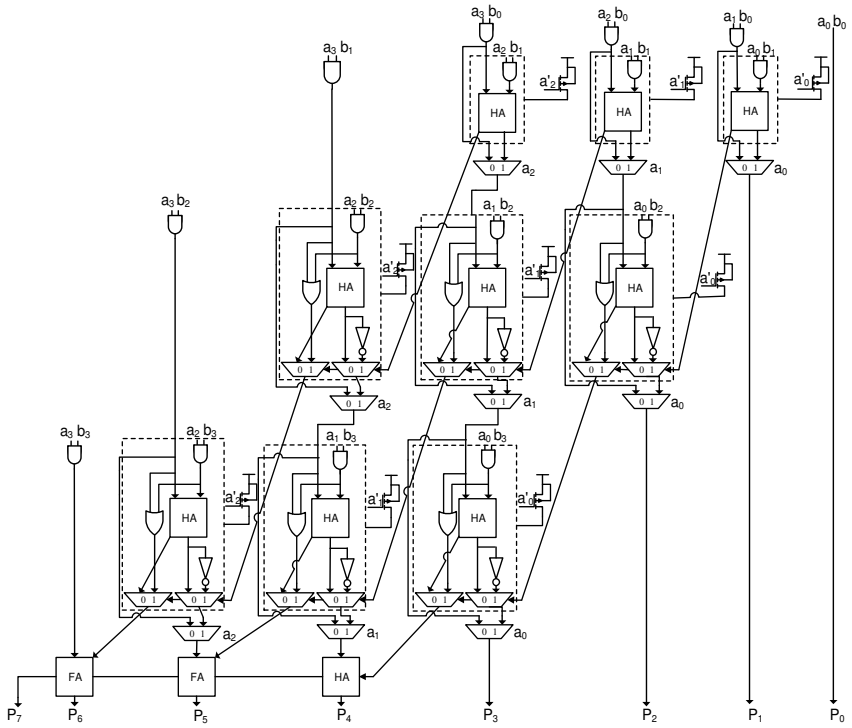


Figure 11. A 4(×)4 Proposed multiplier

Consider the test vectors a = 1100 (as multiplicand) (x) b = 1011 (as multiplier) for the proposed multiplier design. The values on the arrow indicate the value of sum and carry bits as shown in figure 12. In $(j-1)^{th}$ row, initial carry is fixed to zero, it replaces the full adder cells with half adder cells as shown in figure 11. In this row, multiplicand bits a_0 and a_1 are 0, therefore the vectors (a_1b_0) and (a_2b_0) are bypassed to $(j)^{th}$ row by shuting down their respective adder cells with ICBS. In adder cell 3 of $(j-1)^{th}$ row, addition operation is performed by the half adder as the value of multiplicand bit a_2 is 1. It generate sum and carry outputs as 1 and 0 respectively and these outputs are passed to the $(j)^{th}$ row adder cell as shown in figure 12. In the next rows, carry input is may be zero or one. Therefore the logic applied on $(j-1)^{th}$ row is not applicable in succeeding rows. In $(j)^{th}$ row, the carry-in ($C_{i,j-1}$) propagating from $(j-1)^{th}$ controls the addition operation when bypassing scheme is not selected. In this row, a_0, a_1, and carry-in are 0 for adder cell 1 and adder cell 2, therefore, the bypassing operation is performed with ICBS and sum outputs propagating $(j-1)^{th}$ row are selected by multiplexers at the output. For adder cell 3 of $(j-1)^{th}$ row, bypassing is not selected and addition operation is performed by proposed adder cell as multiplicand bit a_2 is 1. Carry-input of this adder cell is 1 and it will control the addition operation. Therefore, the inverter output and OR operation of half adder inputs are selected as final sum (0) and carry (1) outputs by multiplexer of the proposed adder cell at the output. Similar operation is repeated in all successive rows of the multiplier. Finally, 10000100 is obtained as output vectors.

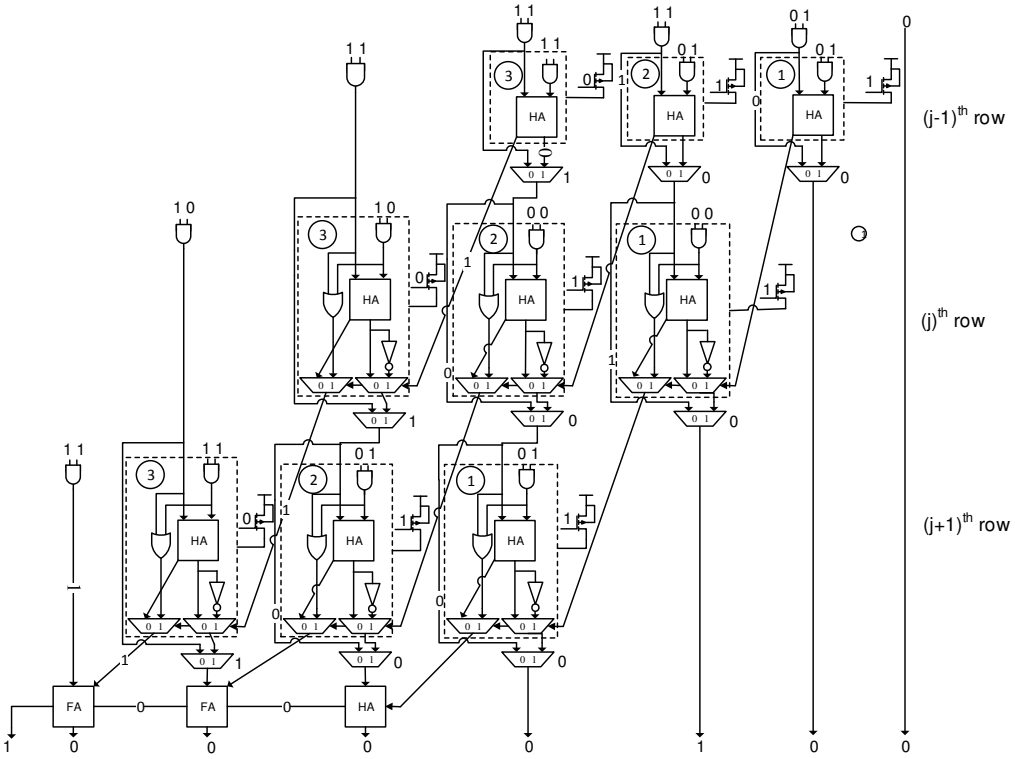


Figure 12. An example of 4(×)4 proposed multiplier

5.RESULTS AND ANALYSIS:

The performance comparison of the proposed multiplier along with the existing multipliers is presented in this section. Performances are compared in terms of power dissipation, worst case dealy, power delay product and area overhead. UMC (United Microelectronics Corporation) 90 nm CMOS technology is adopted to implement the proposed multiplier and existing multipliers using cadence virtuoso tool. Cadence spectre simulator tool is used to estimate the power consumption and worst case delay. Results of proposed multiplier are compared with braun, row bypassing, column bypassing and row and column bypassing multipliers. All the multipliers have been designed for 16 bit and 8 bit multiplication operation. The comparison of power consumption at different operating frequencies ranging from 1 MHz to 333.3 MHz is shown in Table 1. The propagation delay has been calculated for the frequencies ranging from 1 MHz to 333.3 MHz. However the delay of different multiplier at 250 MHz operating frequency is shown in Table 2. The delay is observed from 50% of voltage level of input to 50% of voltage level of resulting output for all the rise and fall transitions. Similarly, comparisons of power delay product for frequencies ranging from 1MHz to 333.3 MHz and area overheads of these multipliers are shown in Table 3 and Table 4. For power delay product, worst case delay is chosen to be the larger delay amongst the all outputs. In this work, the input test patterns are taken randomly with an equal occurrence probability of zero's and one's i.e. the probability of 0 and 1 are 50%.

Table 1

Power consumption (in mW) and power saving

P_{ratio} = Power consumed by the multiplier under consideration

Power consumed by braun multiplier

Multiplier size on different frequency											
Power	Operating frequencies	8 (×) 8 multipliers					16 (×) 16 multipliers				
		Braun	[37]	[10]	[39]	**Proposed**	Braun	[37]	[10]	[39]	**Proposed**
1 Mhz	$P_{consumption}$	0.019	1.585	1.338	1.914	**0.009**	0.113	8.45	7.49	8.792	**0.043**
	P_{ratio}	1	83.42	70.42	100.73	**0.47**	1	74.77	66.28	77.8	**0.38**
2 Mhz	$P_{consumption}$	0.024	1.246	1.269	1.949	**0.011**	0.165	8.219	7.907	8.183	**0.058**
	P_{ratio}	1	51.91	52.87	81.2	**0.45**	1	49.81	47.92	49.59	**0.35**
4 Mhz	$P_{consumption}$	0.035	0.732	0.888	1.549	**0.016**	0.270	6.849	7.609	6.598	**0.087**
	P_{ratio}	1	20.9	25.37	44.25	**0.45**	1	25.35	28.18	24.43	**0.32**
10 Mhz	$P_{consumption}$	0.067	0.353	0.424	0.958	**0.029**	0.585	5.738	7.697	4.646	**0.174**
	P_{ratio}	1	5.26	6.32	14.29	**0.43**	1	9.80	13.15	7.94	**0.29**
50 Mhz	$P_{consumption}$	0.279	0.375	0.362	0.848	**0.117**	2.682	6.072	7.822	4.591	**0.752**

	P_{ratio}	1	1.34	1.29	3.03	**0.41**	1	2.26	2.91	1.71	**0.28**
100 Mhz	$P_{consumption}$	0.543	0.544	0.516	0.926	**0.235**	5.302	7.396	9.083	5.237	**1.469**
	P_{ratio}	1	1.001	0.95	1.70	**0.43**	1	1.39	1.71	0.98	**0.27**
150 Mhz	$P_{consumption}$	0.808	0.722	0.682	1.003	**0.339**	7.93	8.78	10.43	5.923	**2.192**
	P_{ratio}	1	0.89	0.84	1.24	**0.41**	1	1.10	1.31	0.74	**0.27**
250 Mhz	$P_{consumption}$	1.337	1.079	1.018	1.185	**0.559**	13.16	11.57	13.06	7.317	**3.62**
	P_{ratio}	1	0.80	0.76	0.886	**0.41**	1	0.87	0.99	0.55	**0.27**
333.3 Mhz	$P_{consumption}$	1.777	1.378	1.301	1.340	**0.743**	17.52	13.91	15.27	8.486	**4.859**
	P_{ratio}	1	0.77	0.73	0.75	**0.41**	1	0.79	0.87	0.48	**0.27**

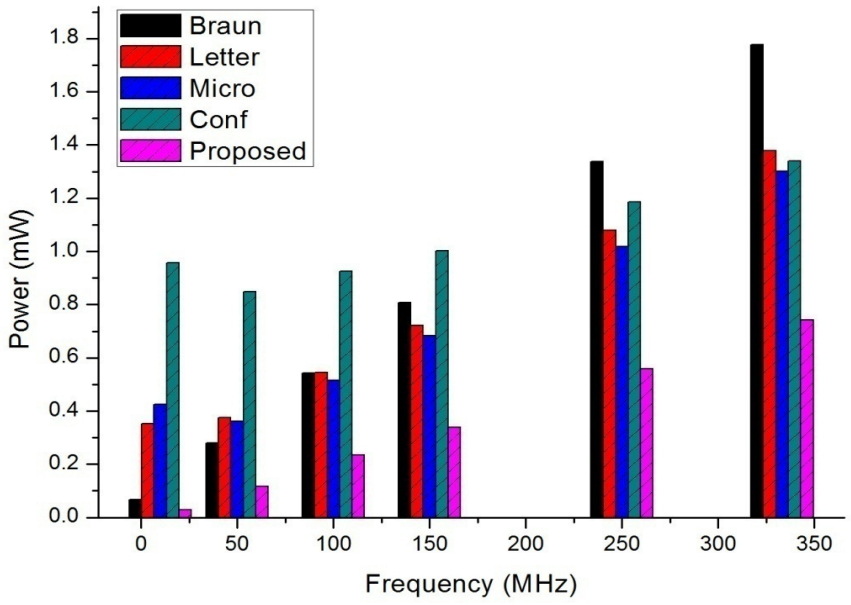


Figure 13. Power comparison of 8(x)8 bit proposed multiplier at different frequencies

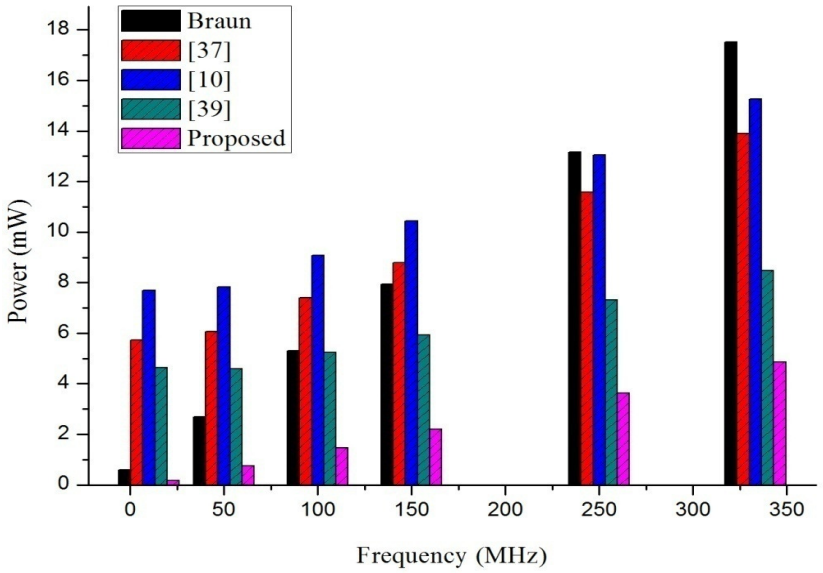


Figure 14. Power comparison of 16(x)16 bit proposed multiplier at different frequencies

Table 2
Delay (in ns) and improvement at 250 MHz frequency

Architecture	Multiplier size and normalized ratio			
	8(×)8	Ratio	16(×)16	Ratio
Braun	1.699	1	2.904	1
[37]	1.459	0.85	2.421	0.83
[10]	1.237	0.72	2.33	0.80
[39]	0.926	0.54	2.007	0.69
Proposed	**1.03**	**0.60**	**2.129**	**0.73**

Table 3

Power-delay product (in pJ) and improvement

$PDP_{ratio=}$ PDP of the multiplier under consideration

PDP of braun multiplier

Multiplier size on different frequency											
Operating frequencies	Power	8 (×) 8 multipliers					16 (×) 16 multipliers				
		Braun	[37]	[10]	[39]	**Proposed**	Braun	[37]	[10]	[39]	**Proposed**
1 Mhz	PDP	0.033	2.312	1.655	1.773	**0.009**	0.328	20.457	17.451	17.645	**0.093**
	PDP_{ratio}	1	70.06	50.15	53.72	**0.27**	1	62.36	53.20	53.79	**0.28**
2 Mhz	PDP	0.042	1.817	1.569	1.805	**0.012**	0.481	19.898	18.423	16.423	**0.124**
	PDP_{ratio}	1	43.26	37.35	42.97	**0.28**	1	41.36	38.30	34.14	**0.25**
4 Mhz	PDP	0.060	1.067	1.099	1.434	**0.016**	0.785	16.581	17.728	13.242	**0.187**
	PDP_{ratio}	1	17.78	18.31	23.9	**0.26**	1	21.12	22.58	16.86	**0.23**
10 Mhz	PDP	0.114	0.515	0.524	0.888	**0.030**	1.700	13.891	17.934	9.324	**0.371**
	PDP_{ratio}	1	4.51	4.59	7.78	**0.26**	1	8.17	10.54	5.48	**0.21**
50 Mhz	PDP	0.474	0.547	0.447	0.785	**0.121**	7.788	14.700	18.225	9.214	**1.602**
	PDP_{ratio}	1	1.15	0.94	1.65	**0.25**	1	1.88	2.34	1.18	**0.20**
100 Mhz	PDP	0.923	0.794	0.639	0.858	**0.242**	15.397	17.905	21.163	10.510	**3.127**
	PDP_{ratio}	1	0.86	0.69	0.92	**0.26**	1	1.16	1.37	0.68	**0.20**
150 Mhz	PDP	1.374	1.053	0.844	0.929	**0.349**	23.028	21.256	24.301	11.887	**4.666**
	PDP_{ratio}	1	0.76	0.61	0.67	**0.25**	1	0.92	1.05	0.51	**0.20**
250 Mhz	PDP	2.271	1.574	1.259	1.097	**0.576**	38.216	28.010	30.429	14.685	**7.706**
	PDP_{ratio}	1	0.69	0.55	0.48	**0.25**	1	0.73	0.79	0.38	**0.20**
333.3 Mhz	PDP	3.019	2.010	1.609	1.241	**0.765**	50.878	33.676	35.579	17.031	**10.344**
	PDP_{ratio}	1	0.66	0.53	0.41	**0.25**	1	0.66	0.69	0.33	**0.20**

Table 4

Total area (in μm^2) and area overhead

Architecture	Multiplier size and normalized ratio			
	8(×)8	Ratio	16(×)16	Ratio
Braun	616.96	1	2626.56	1
[37]	688.96	1.1167	2933.76	1.1169
[10]	678.40	1.099	2913.28	1.109
[39]	499.52	0.809	2121.92	0.807
Proposed	**507.36**	**0.822**	**2177.44**	**0.829**

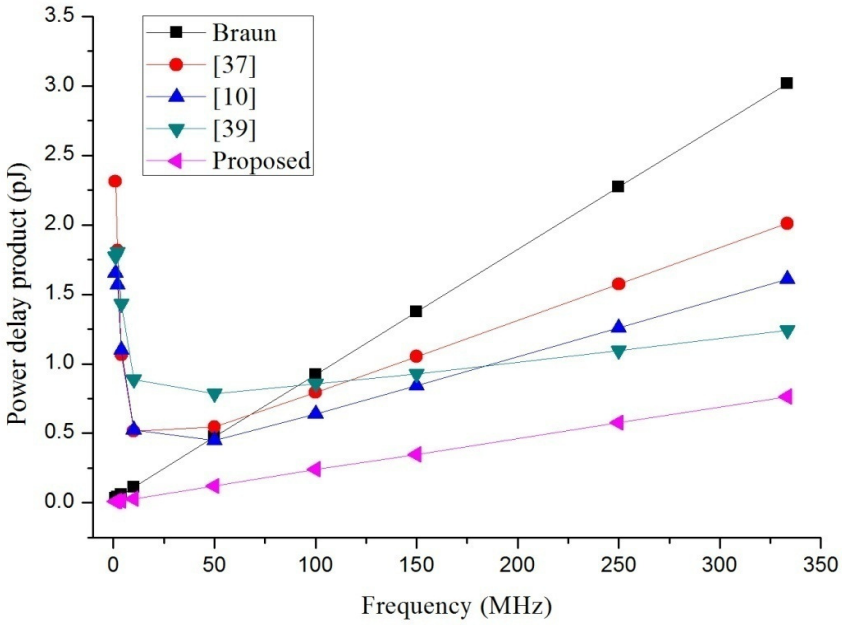


Figure 15. PDP comparison of 8(x)8 bit proposed multiplier at different operating frequencies

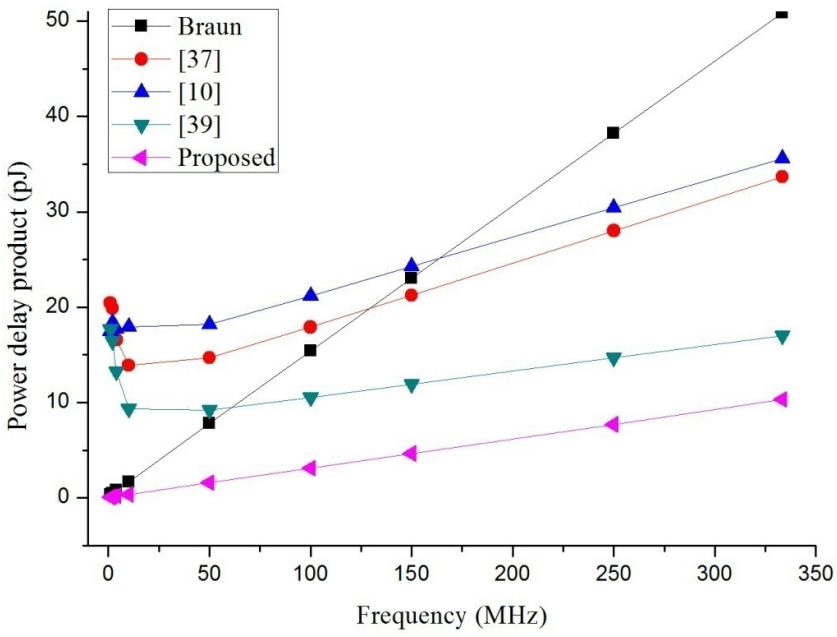


Figure16. PDP comparison of 16(x)16 bit proposed multiplier at different operating frequencies

For 16(×)16 bit multiplier, the proposed design achieves 73 and and 27 percent reduction in power consumption and worst case delay at 250 MHz operating frequency as compared to braun multiplier. Similarly, proposed 8(×)8 bit multiplier achieves 59 and 40 percent reduction in power consumption and worst case delay at 250 MHz operating frequency as compared to braun multiplier. The improvement in power consumption at different operating frequencies of the proposed multiplier as compared to existing multipliers is shown graphically in figure 13 and figure 14. In addition to this, for 16(×)16 bit multiplier, the proposed design achieves 80 percent reduction in power delay product at 250 MHz operating frequency and 17.1 percent reduction in area overhead as compared to braun multiplier. Similarly, proposed 8(×)8 bit multiplier achieves 75 percent reduction in power delay product at 250 MHz operating frequency and 17.8 percent reduction in area overhead as compared to braun multiplier. From the plots, shown in figure 15 and figure 16, it is found that the power delay product of proposed multiplier is much better at low frequencies (≤ 50 MHz) and also better at high frequencies (≤ 333.3 MHz) when compared with existing multipliers. Therefore, the proposed multiplier is a better choice for low frequency applications such as digital hearing aids and also for high frequency applications (≤333.3 MHz) as well.

6.CONCLUSION

A low power, high speed proposed multiplier architecture with improved column bypassing scheme has been presented this work. A new adder with optimized hardware is also proposed. The architecture of this adder reduced the power consumption and propagation delay, when ICBS

is not in use. Simulation results show that the proposed multiplier architecture facilitates reduction of switching transitions and leakage power. It is also found better in terms of area occupancy and propagation delay. While testing, the input test patterns are taken randomly with an equal occurrence probability of zero's and one's. The proposed multiplier can achieve more power saving if the input test pattern has more no. of zero's than the no. of one's. It has been verified that proposed multiplier outperforms previously designed multipliers more effectively at all frequencies and ranks much higher in performance when used for low frequency applications. Therefore, proposed multiplier can be a better choice for assistive listening technology such as hearing aids.

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