A NEW CASCADABLE ADIABATIC LOGIC TECHNIQUE

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ABSTRACT

There are several techniques to realize adiabatic logic but most of them require compliment forms. In this work, a new adiabatic logic technique has been proposed which is capable of working with a single time varying supply voltage. The most attractive feature of the proposed technique is that there is no need of complementary inputs. The proposed adiabatic logic has been implemented by adding charging and discharging paths in the existing standard CMOS logic, using diodes and capacitors. Further, various logic circuits such as INVERTER, NAND, NOR, half adder and positive edge triggered D-flip-flop have been implemented using the proposed adiabatic logic technique. A mathematical expression has been developed to explain the energy dissipation in proposed adiabatic logic technique. All the proposed circuits have been simulated for a time varying supply voltage, peak value of 0.9 Volt. A comparison of these logic circuits designed using 90nm TSMC MOS model, with their standard CMOS based structure shows a large improvement in power consumption to the tune of 60%. The results show that a considerable reduction in power dissipation can be achieved with the proposed adiabatic logic technique and thus we can save significant amount of energy compared to conventional CMOS circuits.

KEYWORDS

Adiabatic Logic, Cascadable Logic, Low power, Energy Recovery Logic Swing, Reversible, dynamic body bias technique.

1.INTRODUCTION

One of the main concerns while designing VLSI circuits is to reduce power dissipation to support higher level of integration of devices on the chip without compromising its reliability. As advancements in battery technology is not able to meet the power requirements, low power techniques are now a necessity due to the heavy usage of high performance hand held devices like notebooks, cell phones and tablets [1,2]. Many low power techniques like altering the input vectors, switching off idle circuits are being used to design low power circuits [3]. Researchers are also exploring many non-conventional techniques for low power design like bulk-driven MOS, floating-gate MOS, quasi floating-gate MOS, body bias technique but these techniques have their own limitations [4,5]. Dynamic threshold MOS is another very attractive option for designing low power circuits operating at voltages lower than 0.7 Volt [6].

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Recently, there is growing interest in adiabatic technique for designing low power VLSI circuits [7]. This technique offers a solution for reduced power dissipation in digital circuits without any circuit complexity. The term "adiabatic" has been taken from thermodynamics which means no exchange of heat with the environment. Adiabatic circuits work on the principle of adiabatic charging and discharging. These circuits recycle the energy from output capacitive nodes instead of discharging it to ground as in conventional CMOS circuits. Adiabatic technique is also termed as Energy Recovery logic due to recycling of energy back to the power source [8]. Thus instead of discharging the capacitor to ground, the charge is discharged to the power supply. Various adiabatic techniques have been proposed in past to overcome increasing power dissipation in VLSI circuits [9].

1.2.Conventional CMOS Logic v/s Adiabatic Logic Technique

Around 80 to 90 per cent of the power dissipation in conventional CMOS circuits is due to charging and discharging of the capacitances. Thus switching power or dynamic power is the most dominant factor in power consumption. However, only 10 to 30 per cent is the leakage power or the static power dissipation and 0 to 5 per cent is short circuit power dissipation. The above mentioned fact indicate that in order to reduce power dissipation significantly, the dynamic power dissipation needs to be reduced. Adiabatic technique provides a way to reduce this dynamic power consumption in the capacitive nodes.

In a conventional static CMOS technique, the energy dissipated across the MOS transistor during charging is ½ CV^2 and the remaining ½ CV^2 is stored in the capacitive node which is being charged. During the discharging of the node, this stored energy is again dissipated across the MOS transistor. Thus a total energy of CV^2 is drawn from the supply voltage given as [10]

$$E_{diss,cmos} = CV^2 \tag{1}$$

In adiabatic technique, a time varying supply voltage is used such that we have a constant current source. The energy dissipated is actually given as [10]

$$E_{diss,adiabatic} = \frac{RC}{T} CV^2 \tag{2}$$

where T is the charging time for the capacitance C and R is equivalent on-resistance of the MOS network.

From Eqs. (1) and (2) it is concluded that by keeping the charging time greater than twice RC the energy dissipated during charging can be made lower than conventional CMOS. In a similar manner the energy stored in the capacitance can be retrieved and sent back to the power supply by changing the direction of the current from the supply voltage. This is the basic principle behind adiabatic charging.

Rest of the paper is organized as follows: section 2 describes the proposed adiabatic logic technique. In section 3 comparison of conventional GFCAL inverter and proposed adiabatic technique based inverter is done. Section 4 briefs about the applications of proposed adiabatic logic technique. Section 5 illustrates the simulation results of the proposed circuits and conclusion is summarized in section 6.

2.PROPOSED ADIABATIC LOGIC TECHNIQUE

In this work, the conventional CMOS based circuit is used to implement the proposed logic and additionally MOS based diodes have been used to make the circuit adiabatic in nature. Figure 1 shows the circuit implementation of the proposed adiabatic logic technique. The proposed adiabatic logic technique uses a single trapezoidal pulse power supply. Here, D1 and D2 are two MOS diodes. D1 is NMOS transistor along the charging path whereas D2 is PMOS transistor along the energy recovery path. This circuit is basically a modified version of diode based adiabatic logic in which the power supply is assumed to be approximately triangular in nature. However, the main limitation of diode based adiabatic logic technique is that amplitude of output degrades and there is a lot of noise due to the leakage current of the diodes. This also results in lower noise margin, reduced output swing and fluctuations in the output. To combat this issue, we have proposed to use capacitors C1 and C2 in charging and discharging paths along with MOS diodes. These capacitors absorb fluctuations and hence fluctuations are reduced to great extent. Additionally, in charging circuitry, we have proposed to use dynamic body bias technique [5] in the MOS diode D1. This helps in increasing the output swing. The static CMOS logic circuit is connected between D1 and D2.

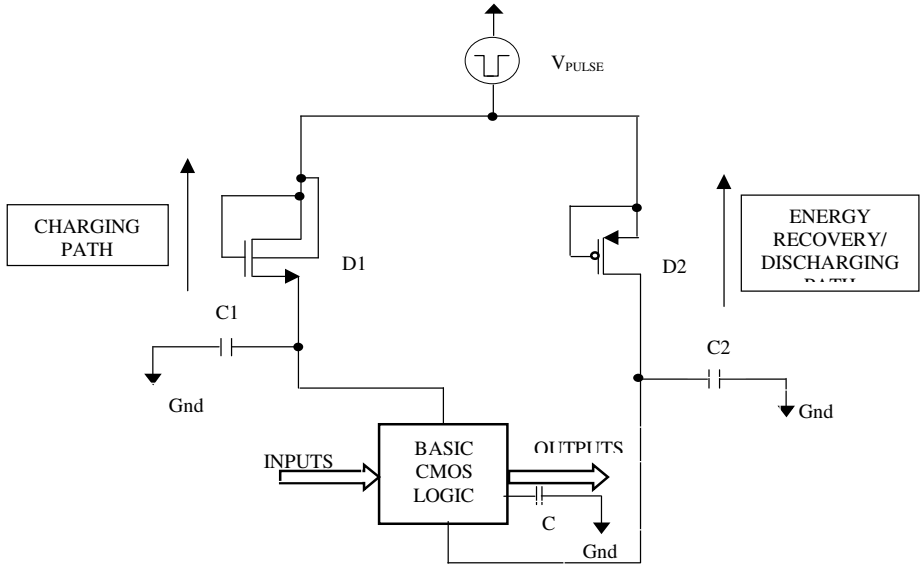

Figure 1. Proposed Adiabatic Logic Technique

3.PROPOSED ADIABATIC INVERTER

A glitch-free and cascadable adiabatic logic (GFCAL) inverter has been proposed in [7] and is shown in figure 2. In this conventional GFCAL inverter, a triangular supply voltage has been used. The capacitor C is charged through MOS transistors M1 and M3 when the input at A is low 'logic 0' during the rising edge of the supply voltage waveform. During the falling edge of the supply voltage M3 is turned off and for a low input at A 'logic 0', the output remains high, if the capacitor is initially charged. The capacitor C is discharged through M4 and M2 transistors when the input logic level at A is high 'logic 1' during the falling edge of the supply voltage waveform. Thus the energy stored in the capacitor is returned to the supply. During the rising edge of the supply and a high logic level at the input, the capacitor remains uncharged as transistor M4 is turned off. The conventional GFCAL mainly suffer from output amplitude degradation, large delay and complex circuit structure. To overcome these limitations, a new adiabatic inverter is proposed as shown in figure 3.

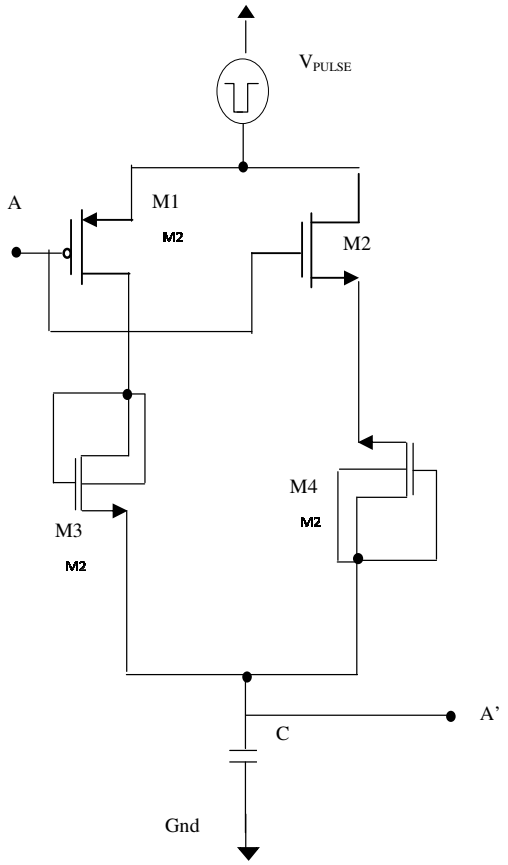

Figure 2. Conventional adiabatic inverter

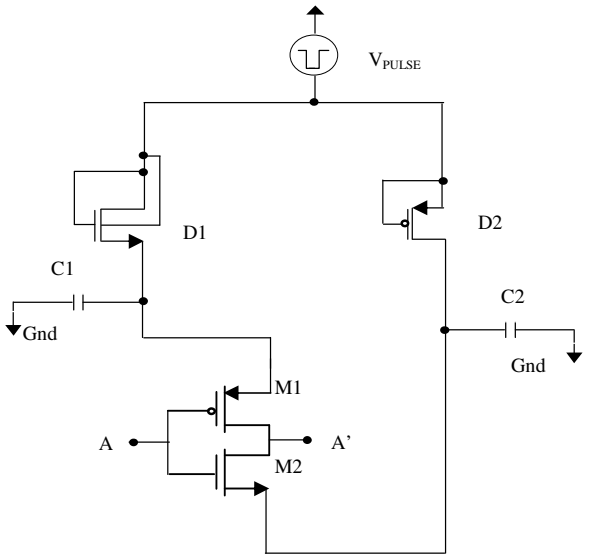

Figure 3. Proposed adiabatic inverter

The proposed adiabatic inverter circuit is powered by a trapezoidal power supply and the static CMOS inverter is connected between the charging transistor D2 and the discharging diode D1. Suppose the output capacitance at node A' is uncharged and the input at node A is logic '0'. Due to logic '0' at the input M1 transistor turns on and as the supply exceeds the cutin voltage Vtn of diode D1, it turns on and inverter output node A' charges through D1 and M1. Thus a low input gives a high output. When the output capacitance at node A' is in charged state and the input at node A is logic '1'. The high input level will turn on transistor M2 and D2 turns on as soon as the supply exceeds the cutin voltage Vtp of the diode D2. Thus the output node capacitance discharges through M2 and D2 and the charge is sent back to the power supply.

When the output capacitance at node A' is charged and the input is at logic low level '0'. Here M2 transistor will not turn on and thus the discharge path for output node back to the power supply is cut through M2 and hence the output capacitance does not discharge and the high output level is maintained. When the output capacitance node A' is uncharged and the input at node A is logic '1', transistor M1 will not turn on and the charging path via D1 is not completed, thus the output node remains at logic low level.

In the last two cases it can be observed that dynamic switching does not take place hence power dissipation is reduced. The energy dissipated in the proposed inverter is calculated using the approximate expression derived by the authors.

(a) Energy dissipation during charging

During the ON duration of the PMOS transistor in static CMOS inverter, since V_{DD} increases from 0 to V_0, the load capacitor C is charged through the capacitor C1 and diode D1 in the

charging path shown in Fig.3.The voltage reaches a peak value V_0 in a time period T and its value $V_{DD}(t)$ at any time 't' is therefore given by Eq.(3) and Eq.(4).

$$V_{DD}(\mathrm{t}) = V_0 \frac{t}{T} \text{ when } 0 \leq t \leq T \quad \text{and} \tag{3}$$

$$= V_0[1 - \frac{(\mathrm{t-T})}{T}] \text{ when } \mathrm{T} \leq t \leq 2T \tag{4}$$

The voltage $V_{DD}(t)$ reaches a value V_B in a period T_{ch}, when the conduction of the diode starts. Let R_{ch} be the total resistance in the charging path.

The voltage V_C across the load capacitor 'C' for $t>T_{ch}$, is given as

$$\frac{V_0}{T}\mathrm{t} = V_B + R_{ch}\frac{C_1 C}{C_1+C}\frac{dV_c}{dt} + V_c \tag{5}$$

Assuming that $T_{ch} > \frac{C_1 C}{C_1+C} R_{ch}$, solving Eq.(5), Energy E_{ch} dissipated over the period 0 – T in the diode, capacitor C_1 and the transistor is obtained as

$$E_{ch} \approx V_0 \frac{C_1 C}{C_1+C}\left(R_{ch}\frac{C_1 C}{C_1+C}\frac{V_0}{T} + V_B\right)\left(1 - \frac{V_B}{V_0}\right) \tag{6}$$

(b) Energy dissipation during discharging

When the PMOS is OFF and the NMOS transistor in static CMOS inverter is ON, charging of the load capacitor is prevented and it starts discharges through the diode and capacitor C_2 in the discharge path till t_{dc} i.e, till V_C is higher than the supply voltage by at least V_B, when V_{DD} increases from 0 to V_0. The capacitor then stops discharging at t_{dc} and again continues discharging from $2T - t_{dc}$ until $V_C = V_B$. Let R_{dis} be the total resistance in the discharging path. Assuming $CR_{dis} < t_{dc}$, the energy E_{dc} dissipated during discharging is the sum of energy dissipated during 0 to t_{dc} and $(2T - t_{dc})$ to $2T$ which is obtained as

$$E_{dc} \approx t_{dc}\left(2\frac{V_0^2}{T^2}\left\{\frac{C_2 C}{C_2+C}\right\}^2 R_{dis}\right) - 2\frac{C_2 C}{C_2+C}\frac{V_0}{T}B\frac{C_2 C}{C_2+C}R_{dis} + V_B B\frac{C_2 C}{C_2+C} + \frac{\mathrm{B}^2}{2}\frac{C_2 C}{C_2+C} \tag{7}$$

where $B = V_{C0} - V_B + R_{dis}\frac{C_2 C}{C_2+C}\frac{V_0}{T}$

The total energy E_D, dissipated during one cycle of charging and discharging is given as

$$E_{diss,adiabatic,p} = E_{ch} + E_{dc} \tag{8}$$

Further on substituting values of E_{ch} and E_{dc} from Eq.(6) and Eq.(7) respectively in Eq.(8), we get

$$E_{diss,adiabatic,p} = V_0 \frac{C_1 C}{C_1+C}\left(R_{ch}\frac{C_1 C}{C_1+C}\frac{V_0}{T} + V_B\right)\left(1-\frac{V_B}{V_0}\right) + t_{dc}\left(2\frac{{V_0}^2}{T^2}\left\{\frac{C_2 C}{C_2+C}\right\}^2 R_{dis}\right) - 2\frac{C_2 C}{C_2+C}\frac{V_0}{T} B \frac{C_2 C}{C_2+C} R_{dis} + V_B B \frac{C_2 C}{C_2+C} + \frac{B^2}{2}\frac{C_2 C}{C_2+C} \quad (9)$$

where t_{dc} is given by

$$t_{dc} = R_{dis}\left(\frac{C_2 C}{C_2+C}\right) \ln\left[\frac{V_{C0} - V_B + \left(R_{dis}\frac{C_2 C}{C_2+C}\frac{V_0}{T}\right)}{R_{dis}\left(\frac{C_2 C}{C_2+C}\right)\frac{V_0}{T}}\right] \quad (10)$$

Thus Eq.(9), gives the theoretical expression for energy dissipation during charging and discharging cycles for the proposed circuit, it can therefore be implied from this equation that as T increases, the energy dissipation decreases. Here, T indicates the rate of variation of the supply. Also, this equation indicates that the power dissipation generally changes with capacitance values, V_0, slowly varying supply voltages and the equivalent series resistance due to MOS and diode.

4. APPLICATIONS OF PROPOSED ADIABATIC LOGIC TECHNIQUE

The proposed adiabatic logic technique in section 2 has been used to design various adiabatic circuit applications such as NAND gate, NOR gate, Half adder and D flip flop. The structure of proposed NAND and NOR gate is shown in figure 4 and figure 5 respectively.

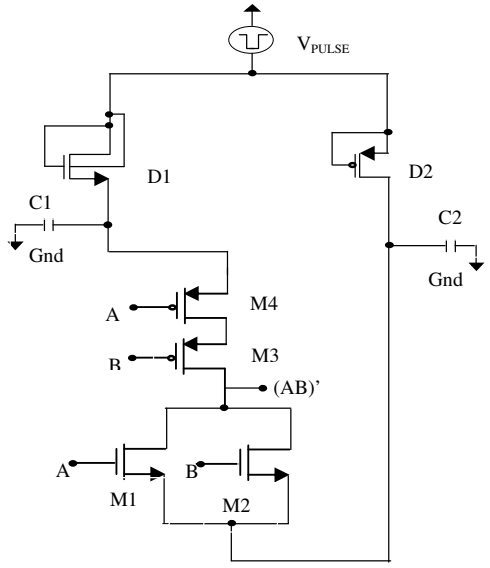

Figure 4. Proposed adiabatic NAND gate

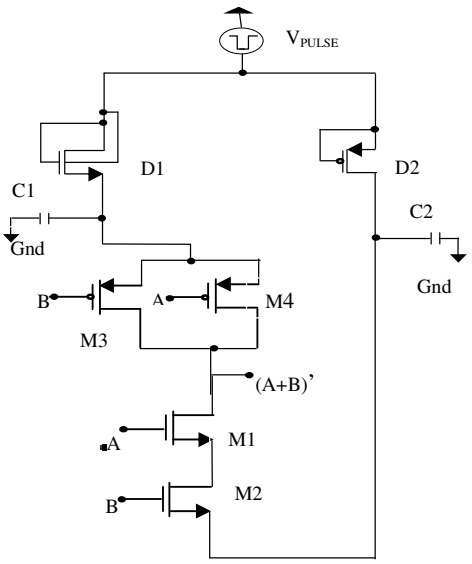

Figure 5. Proposed adiabatic NOR gate

The structure of proposed half adder is shown in figure 7. It consists of one XOR gate and one AND gate. The XOR gate has been implemented using two NOR gates and one AND gate as shown in figure 6. In this figure, the AND gate is implemented by connecting the output of a NAND gate as input to the inverter. The OR gate is implemented by connecting the output of a NOR gate as input to the inverter.

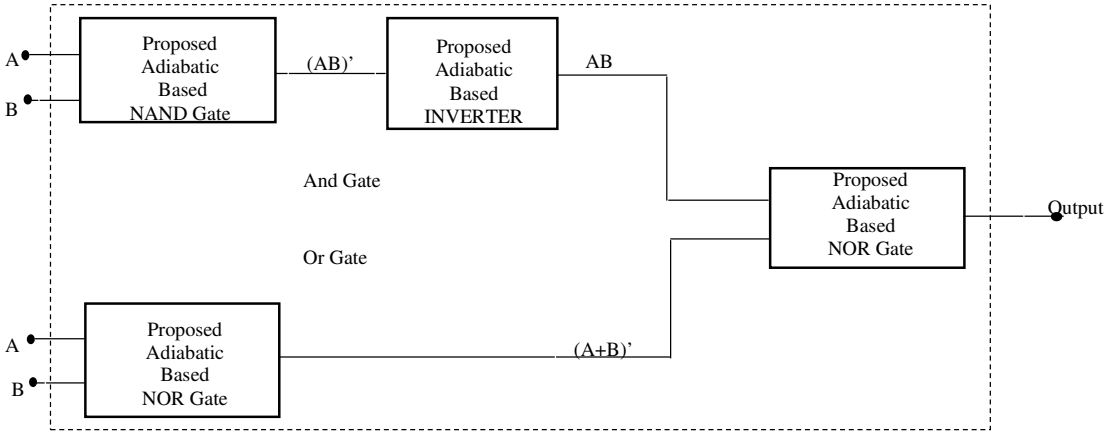

Figure 6. Proposed adiabatic XOR gate

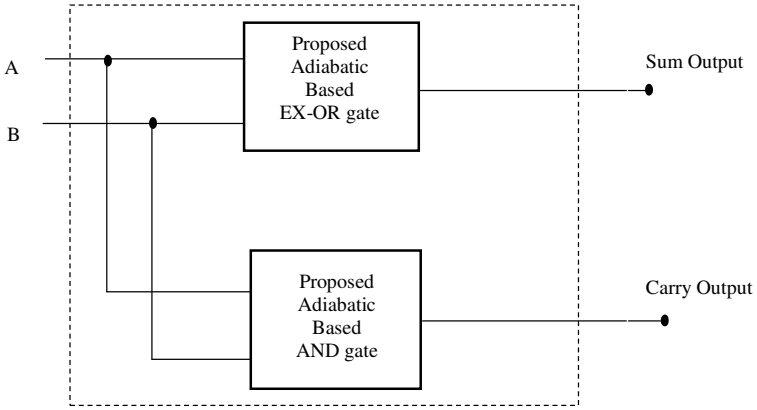

Figure 7. Proposed adiabatic Half-Adder

The structure of proposed Positive edge D Flip-flop is shown in figure 8. It consists of five two input and one three input NAND gates. When the clock is enabled, the output changes according to the D input, that is, outputs Q='1' and Q'='0' when D='1'. Similarly, Q = '0' and Q'= '1' when D='0'.

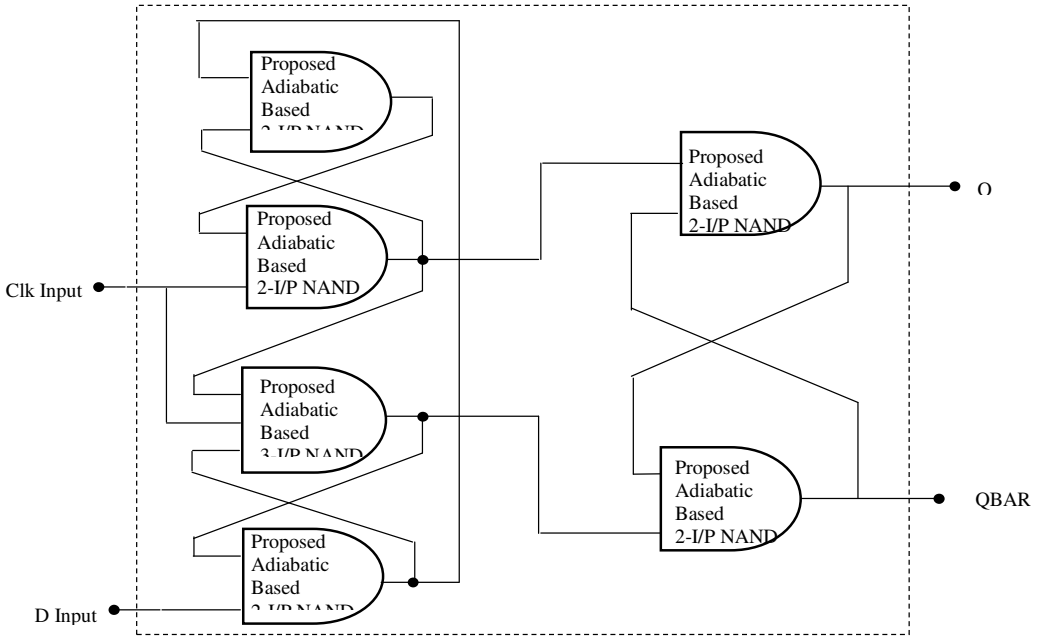

Figure 8. Proposed adiabatic D Flip-flop

5.SIMULATION RESULTS

All the proposed circuits have been designed using 90 nm TSMC MOS model and simulated at 0.9 Volt of trapezoidal power supply. The capacitors C1 and C2 are 1nF each. The length and width of each transistor is 0.09 um and 1.8 um respectively. The simulated result of conventional adiabatic inverter is shown in figure 9 corresponding to the input string "01010101". There is a non-ideality in the output of this inverter which is not desirable.

Figure 10 shows the output of the proposed adiabatic inverter corresponding to the input string "01010101". It is very clear from the simulation result of proposed adiabatic inverter that the output swing is equal to the input swing and also the glitch in conventional inverter output has been eliminated.

As the, output logic level in proposed inverter is nearly the same as that of input logic levels i.e, 0V for logic '0' and 0.9 Volts for logic '1', therefore, cascaded logics can be implemented using this proposed adiabatic technique very comfortably with desired logic swing.

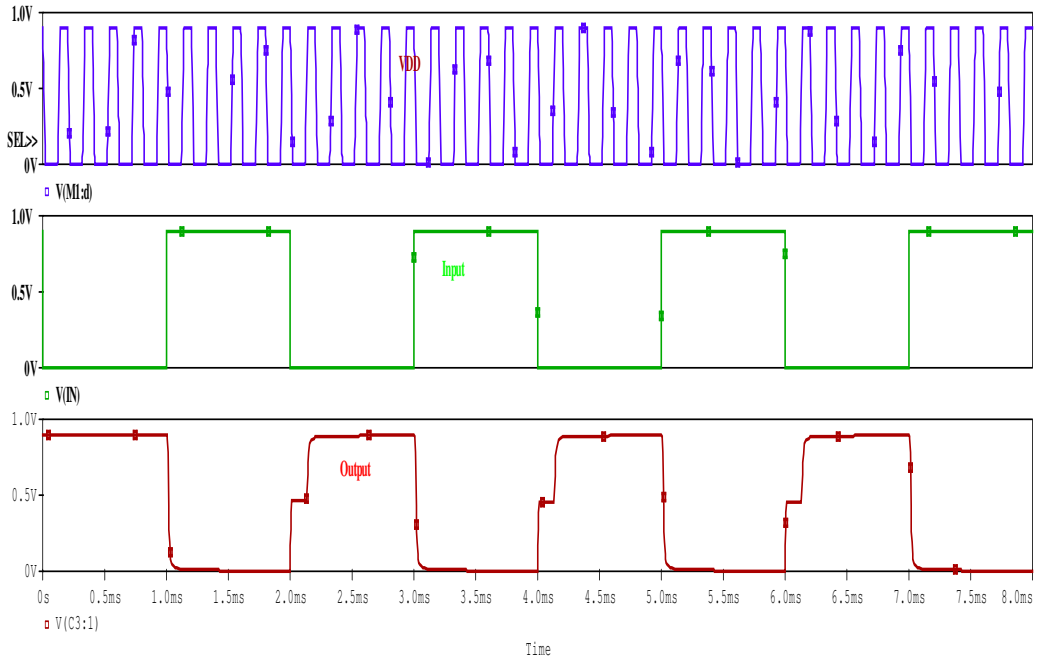

Figure 9. Waveforms for conventional adiabatic inverter
(x axis: time and y axis: 1st – VDD , 2nd – Input A, 3rd – Inverted Output(A)')

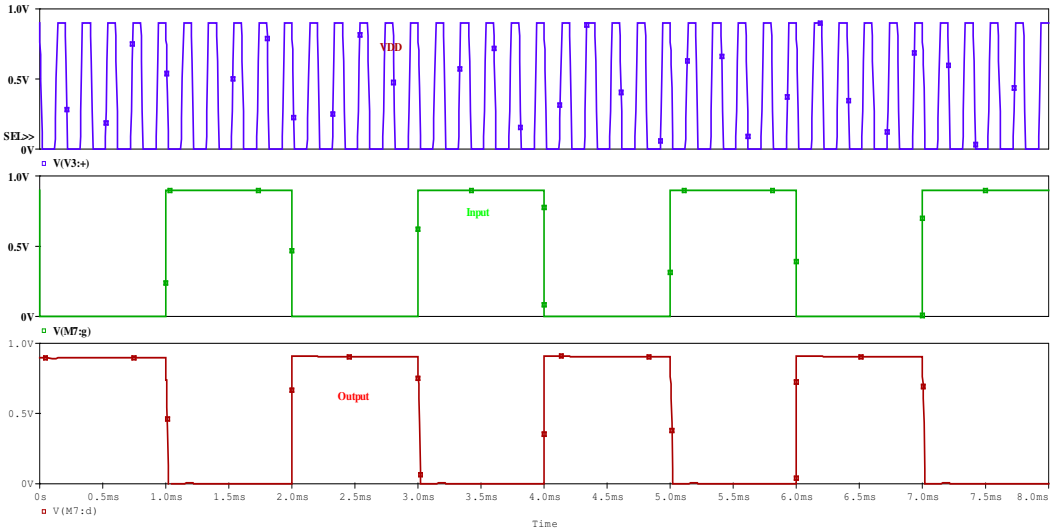

Figure 10. Waveforms for proposed adiabatic inverter
(x axis: time and y axis: 1st – VDD , 2nd – Input A, 3rd – Inverted Output (A)')

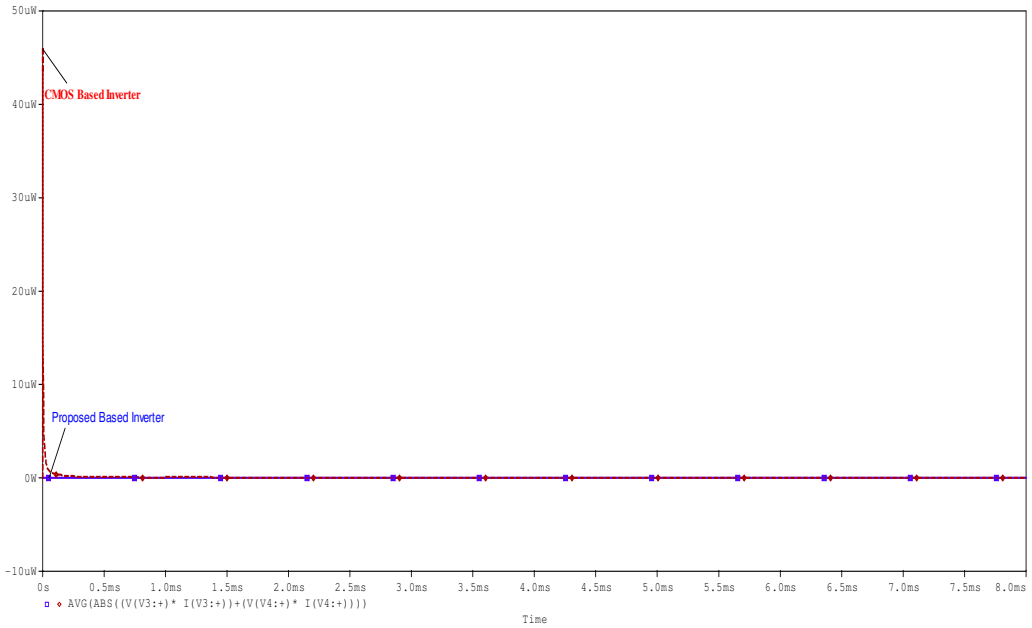

Figure 11. Comparison of power dissipation for the static CMOS inverter and proposed adiabatic inverter
(x axis: time and y axis: Power dissipation)

Figure 11. shows the comparison of power dissipation in proposed adiabatic inverter as compared to static CMOS inverter. It is observed from this result that the proposed adiabatic inverter power dissipation has been reduced considerably as compared to the static CMOS inverter. Table 1 summarizes the power dissipation in conventional adiabatic inverter, proposed adiabatic inverter and static CMOS inverter. It is observed from the table that proposed adiabatic logic technique has reduced the power consumption in proposed inverter by 60% as compared to conventional adiabatic inverter.

Figure 12. shows the simulated output of the proposed adiabatic NAND gate corresponding to the input string "01010101" and "00110011". The output corresponding to the above mentioned inputs comes out to be "11101110".

Figure 13. shows the output of the proposed adiabatic NOR gate corresponding to the input string "01010101" and "00110011". The output corresponding to the above mentioned inputs comes out to be "10001000".The proposed logic is so sensitive that it can capture even the sharp changes in the input and corresponding glitch can be seen in the output where there is a sharp change of input from 0→1 or 1→0. This can be useful in applications needing high sensitivity of output towards input.

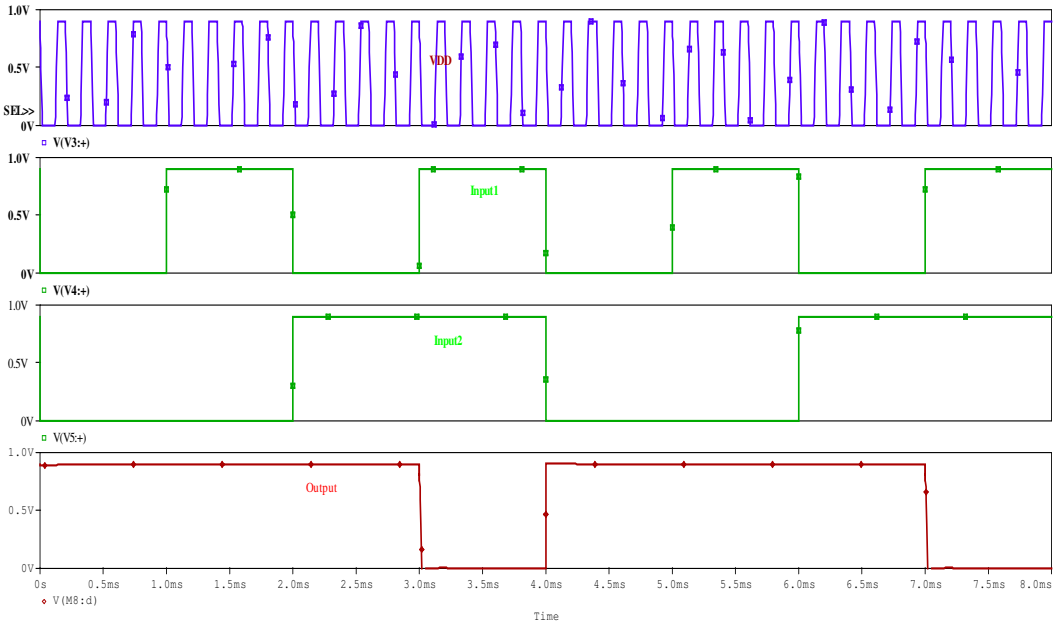

Figure 12. Waveforms for the proposed NAND gate
(x axis: time and y axis: 1st – VDD , 2nd – Input A, 3rd – Input B, 4th – Output(A+B)')

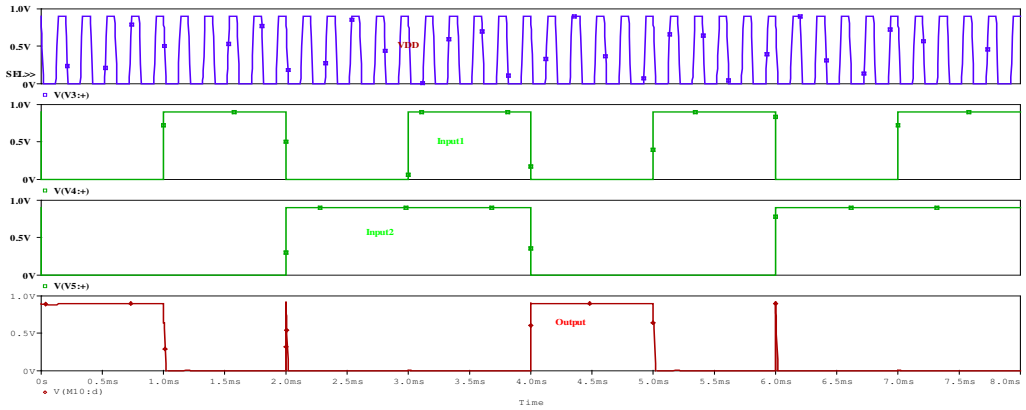

Fig.13: Waveforms for the proposed NOR gate
(x axis: time and y axis: 1st – VDD , 2nd – Input A, 3rd – Input B, 4th– Output(AB)')

Figure 14. shows the output of the proposed adiabatic half adder corresponding to the input string "01010101" and "00110011". The sum output corresponding to the above mentioned inputs comes out to be "01100110" and the carry output corresponding to the above mentioned inputs comes out to be "10001000" as expected.

Figure 15. shows the output of the proposed adiabatic positive D-Flip Flop corresponding to the D input string "010101". The initial fluctuations in the output are due to the setup time constraints and after that the output is stable from 1.5ms and we get the desired output i.e, the output changes according to D-input when positive edge of clock arrives. Table 2 summarizes the power dissipation in proposed adiabatic NAND gate, NOR gate, half adder and positive edge D flip flop as compared to their static CMOS counterparts. It is observed from the table that proposed adiabatic logic technique has reduced the power consumption significantly in the proposed circuits.

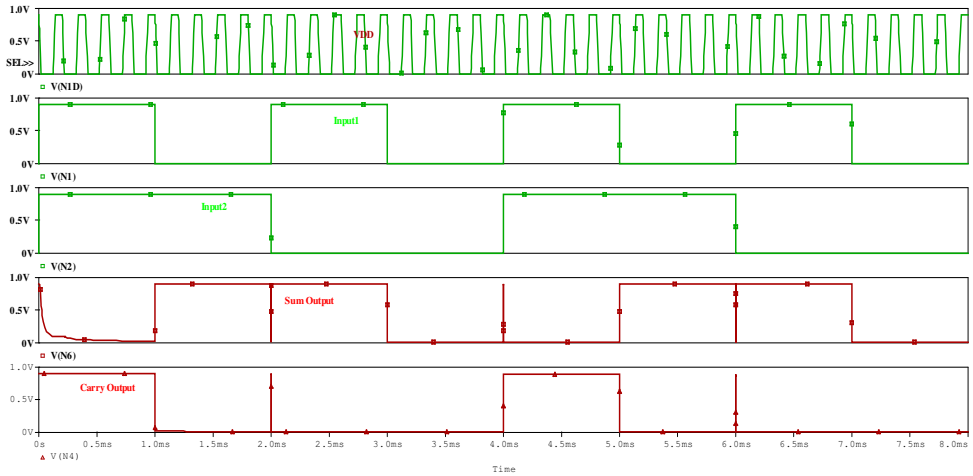

Figure 14. Waveforms for the proposed Half Adder
(x axis: time and y axis: 1st – VDD , 2nd – Input A, 3rd – Input B, 4th– Sum Output, 5th– Carry Output)

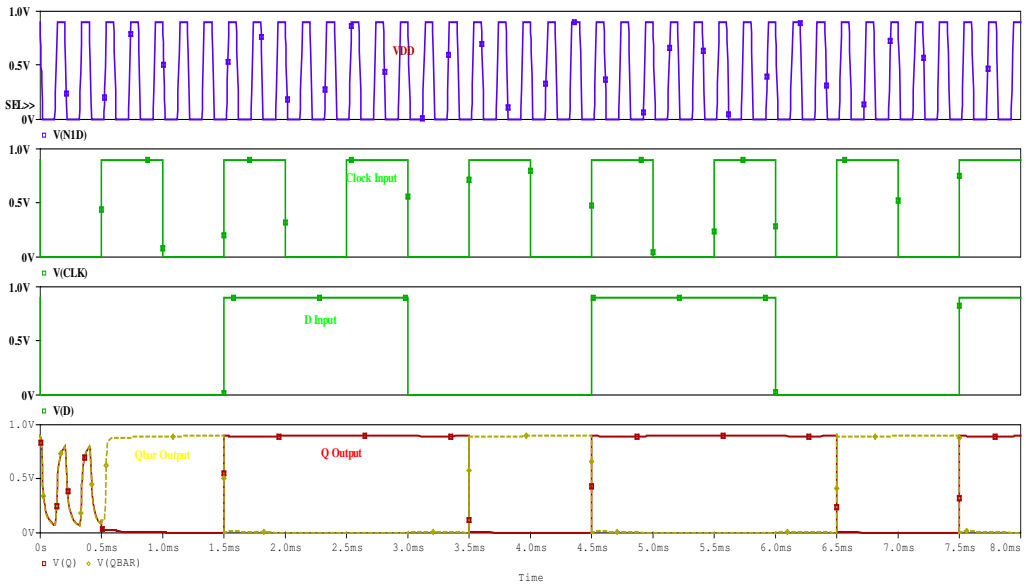

Figure 15. Waveforms for the proposed D Flip-Flop
(x axis: time and y axis: 1st – VDD , 2nd – Clk Input, 3rd – Input D, 4th – Q Output(—) and Q' Output (- - -))

Table 1. Comparison of power dissipation of inverter circuits

Circuit	Power Dissipation (in W)
CMOS inverter	46.11u
GFCAL inverter	133.33n
Proposed inverter	53.33n

Table 2. Comparison of power dissipation of NAND gate, NOR gate, half adder and positive edge D flip flop circuits

Proposed Circuit	Power dissipation using proposed adiabatic logic technique (in W)	Power dissipation using static CMOS logic (in W)
NAND Gate	4.0231n	62.716u
NOR Gate	4.0578n	70.636u
Half adder	135.69u	154.451u
D Flip-Flop	84.39u	141.763u

6. CONCLUSION

In this paper a new cascadable adiabatic logic technique has been proposed. This technique provides considerable reduction in power dissipation compared to conventional adiabatic circuit to the tune of 60%. A significant amount of power reduction has been achieved reduction in proposed applications of new adiabatic logic technique. There is no degradation in the amplitude of output voltage and therefore proposed circuits in this work can be used in designing cascaded structures. All the proposed circuits have been simulated in SPICE with 90 nm technology node. These circuits are well suited for ultra low power circuit applications.

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