SINGLE PHASE SYMMETRICAL MULTILEVEL INVERTER DESIGN FOR VARIOUS LOADS

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ABSTRACT

This paper presents a single phase symmetrical multilevel inverter with various loads. This proposed topology is connected with R-load, RL-load and induction motor drive with unipolar Phase disposition PWM technique. Among the four modulation technique it gives reduced harmonic. This proposed topology has less number of switches than the conventional one. In conventional cascaded multilevel inverter have twelve switches and the proposed topology have eight switches. Totally the four switches have been reduced from the conventional one. It is designed to produce a seven level output. The simulation analysis has been done by a MATLAB/SIMULINK model.

KEYWORDS

Total Harmonic Distortion, Pulse Width Modulation, Cascaded multilevel inverter, Induction Motor.

1. INTRODUCTION

MLIs have been drawing growing attention in the recent years especially in the distributed energy resources area because several batteries, fuel cells, solar cells or rectified wind turbines or micro turbines can be connected through a MLI to feed a load or interconnect to the AC grid without voltage balancing problems. The unique structure multilevel VSIs allow them to reach high voltages with low harmonics without the use of transformers. This makes these unique power electronic topologies suitable for FACTS and custom power applications. The unique structure multilevel VSIs allow them to reach high voltages with low harmonics without the use of transformers. This makes these unique power electronic topologies suitable for FACTS and custom power applications. Holmes et al [1] introduced opportunities for Harmonic Cancellation with Carrier Based PWM for two level and multilevel cascaded inverters. Rodriguez et al [2] this paper presents the most relevant control and modulation methods developed for this family of converters multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation Li et al [3] proposed a real time testing of a controller for multi bus micro grid system. Tallam et al [4] introduced a carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters. Leppanen et al [5] suggested the observer using low-frequency Injection for Sensor less Induction Motor Control-Parameter Sensitivity Analysis. McGrath et al [6] proposed a new multilevel inverter shows reduction in the total harmonics upto 60 percentage.Rodriguez et al [7] proposed multilevel voltage source converter topologies for industrial medium voltage drives. Zhong et al [8] deals with a DC-AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications. Lezana et al [9] describes a survey on fault operation on multilevel inverters.

Malinowski et al [10] describes a survey on cascaded multilevel inverters. Sepahvand et al [11] developed a capacitor voltage regulation in cascaded H-bridge multilevel converters with fundamental frequency switching. Ehsan Najafi et al [12] proposed a new multilevel inverter topology with various carrier based techniques and the various analysis also done for this topology. Balamurugan et al [13] presents various PWM techniques and the IM gives the fewer harmonic compared to other techniques. Saipadhma et al [14] deals with the voltage control strategy fundamental switching and Sinusoidal Pulse Width Modulation of the conventional cascaded inverter topology is compared with the new reverse voltage topology. Srinivas Reddy Chalamalla [15] introduced a new technique with an induction motor drive which produces a low switching frequency.

2. CASCADED MULTILEVEL INVERTER

The problem of eliminating harmonics in inverter has been focus of research for many years. To reduce the harmonics different multilevel SPWM and SVPWM schemes are suggested in the literature however these PWM techniques increase the control complexity and switching frequency. In selective harmonic elimination or programmed harmonic elimination method the switching angles are chosen or programmed to eliminate specific harmonics. The power circuit Fig.1 consists of a cascade of N independent single-phase inverters. Using the top FBI as the example, turning on S_{11} and S_{41} yields $+V_{dc}$ output. Turning on S_{21} and S_{31} yields $-V_{dc}$ output. Turning off all switches yields 0 volts output. The AC output voltage at other FBIs can be obtained in the same manner. The number of voltage levels at the load generally defines the number of FBIs in cascade. The number of FBI units or DC sources N is (m-1)/2 where m is the sum of zero level and the number of positive and negative levels in MLI output. Each switching component turns on and off only once per cycle i.e. at the line frequency. The main features of cascaded multilevel inverters are:

- It can generate almost sinusoidal output voltage while switching only one time per fundamental cycle.
- It can eliminate transformers of multi-pulse inverters used in conventional utility interfaces and static VAR compensators.

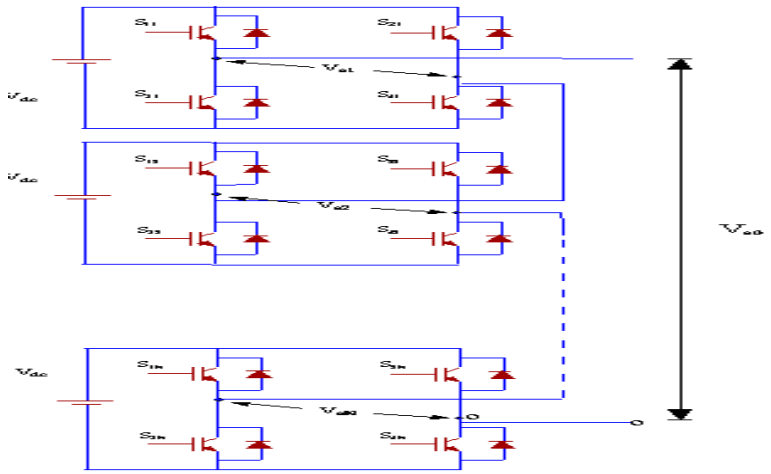

Figure 1. Cascaded H-bridge multilevel inverter

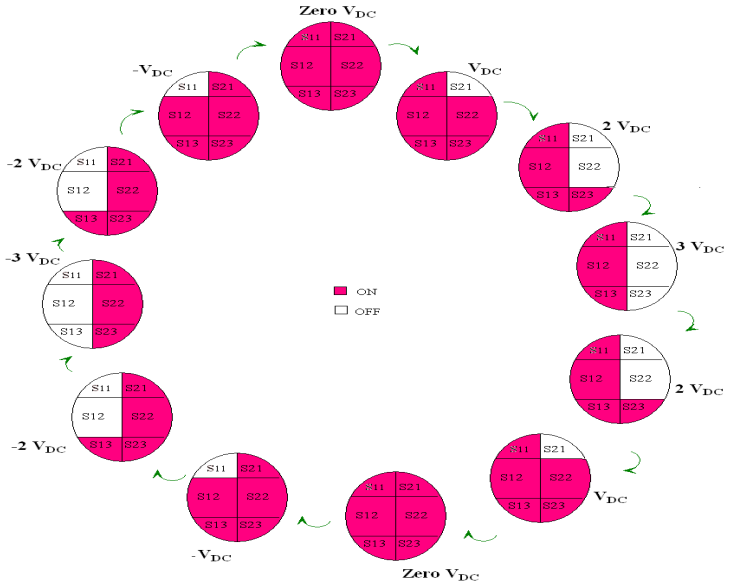

Figure. 1 (a) Cyclic switching sequence of chosen seven level inverter

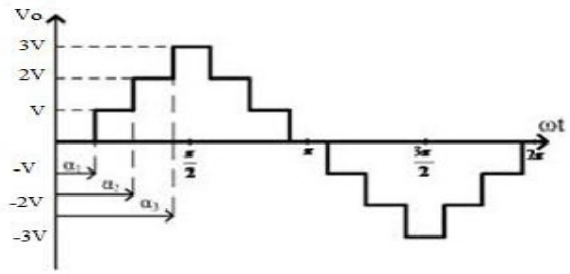

Fig. 1 (b) Output of cascaded multilevel inverter

3. PROPOSED MULTILEVEL INVERTER

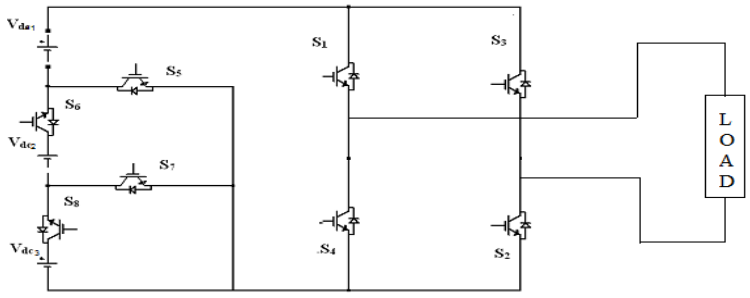

Figure 2. Proposed seven level inverter with load.

Fig. 2 shows the proposed seven level inverter circuits. This proposed method is different from the method since it does not have any bidirectional switch and different from the method since it has less number of switches.

PWM techniques are employed in inverters to achieve high quality output voltage of desired amplitude and frequency which are as close as possible to sinusoidal wave. Power electronics researchers have many control techniques to reduce harmonics in such cases. Table 1 shows the switching pattern.

Table 1. Switching table for proposed multilevel inverter.

S1	S2	S3	S4	S5	S6	S7	S8	Output V
1	1	0	0	0	1	0	1	$+3V_{dc}$
1	1	0	0	0	1	1	0	$+2V_{dc}$
1	1	0	0	1	0	0	0	$+V_{dc}$
0	0	0	0	0	0	0	0	$0V_{dc}$
1	1	0	0	1	0	0	0	$- V_{dc}$
1	1	0	0	0	1	1	0	$-2V_{dc}$
1	1	0	0	0	1	0	1	$-3V_{dc}$

4. SIMULATION OUTPUT AND RESULTS

The MATLAB simulation circuit was developed for proposed seven levels inverter with various loads.

4.1. Proposed Circuit With R-Load

The circuit consists of 12 switches with three equal dc sources. The load has been used as a resistive load. In the SIMULINK circuit pulses are generated by using pulse generators only. For each H-bridge two pulses are generated for two pairs of switches. This means that two opposite switches in each H-bridge is turned ON and OFF at the same instant of time. The simulation circuit for a proposed multilevel inverter with R load has been shown below. By using this

simulation circuit the harmonics and output voltage analysis has been done. It has been shown in below figure 4 and 5.

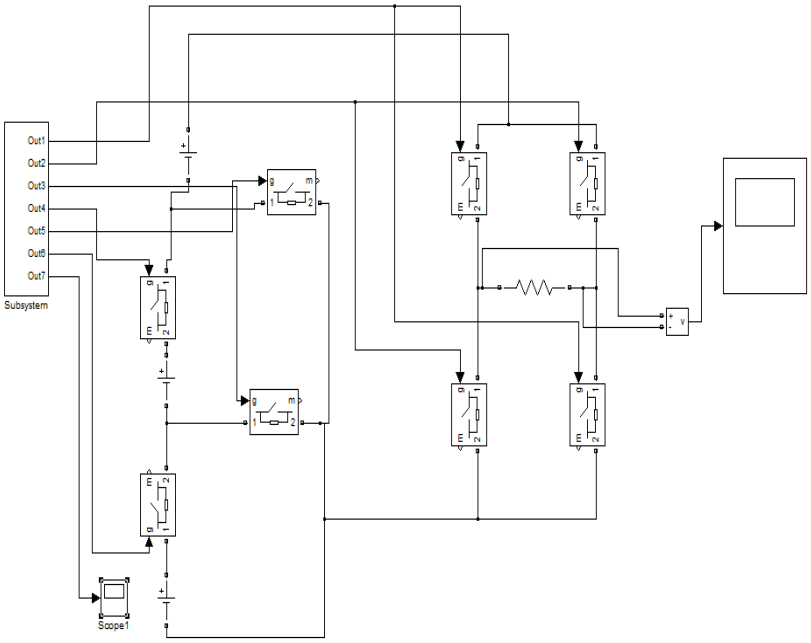

Figure 3. Simulation circuit for a cascaded H-bridge MLI fed with R load.

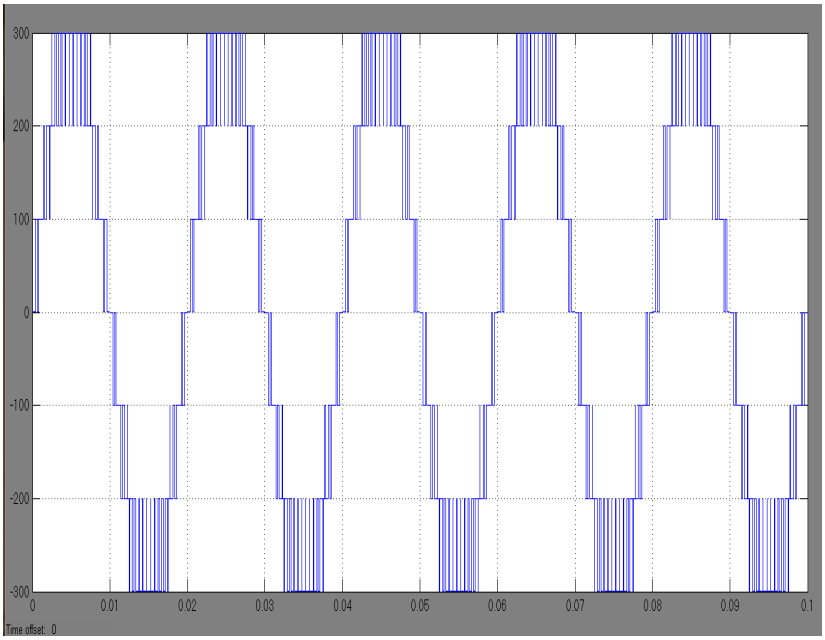

Figure 4. Output voltage of proposed inverter with R-load

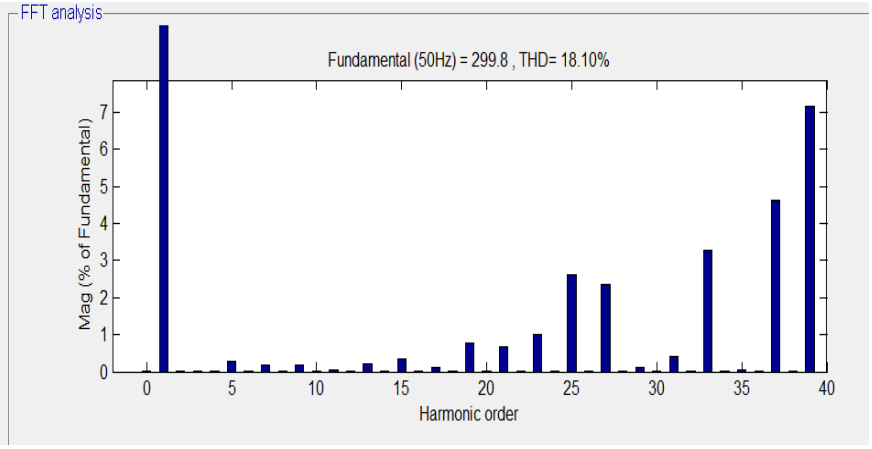

Figure 5. Harmonic spectrum of output voltage of the proposed inverter with R-load

3.2. Proposed circuit with RL-load

The proposed circuit consist of RL load in a output side of a simulation circuit. This simulation circuit is used to analyse the harmonics and the output voltage. Fig. 6 to 8 shows the sample simulink model, output voltage and FFT plot.

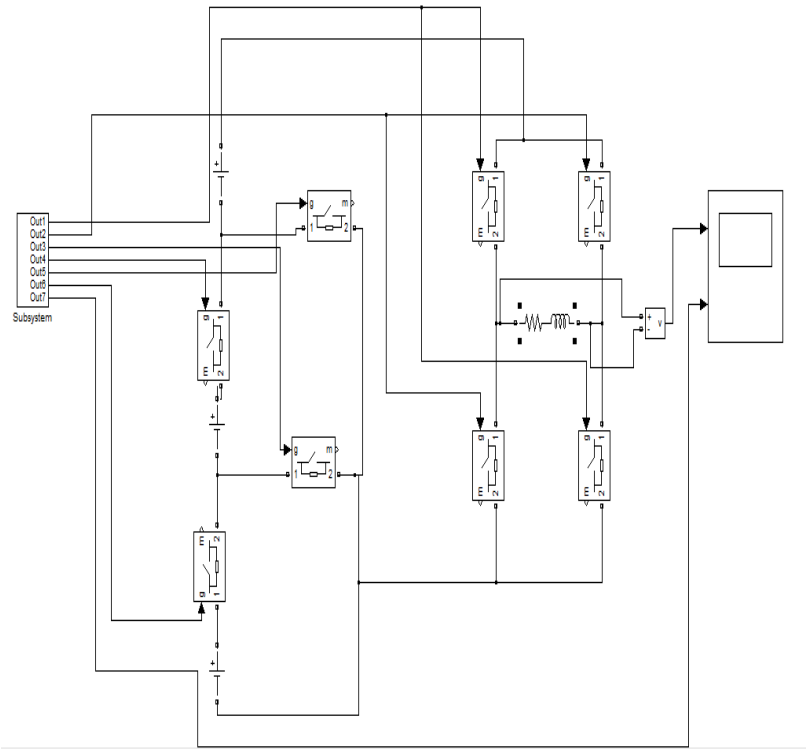

Figure 6. Simulation circuit for a cascaded H-bridge MLI fed with RL load

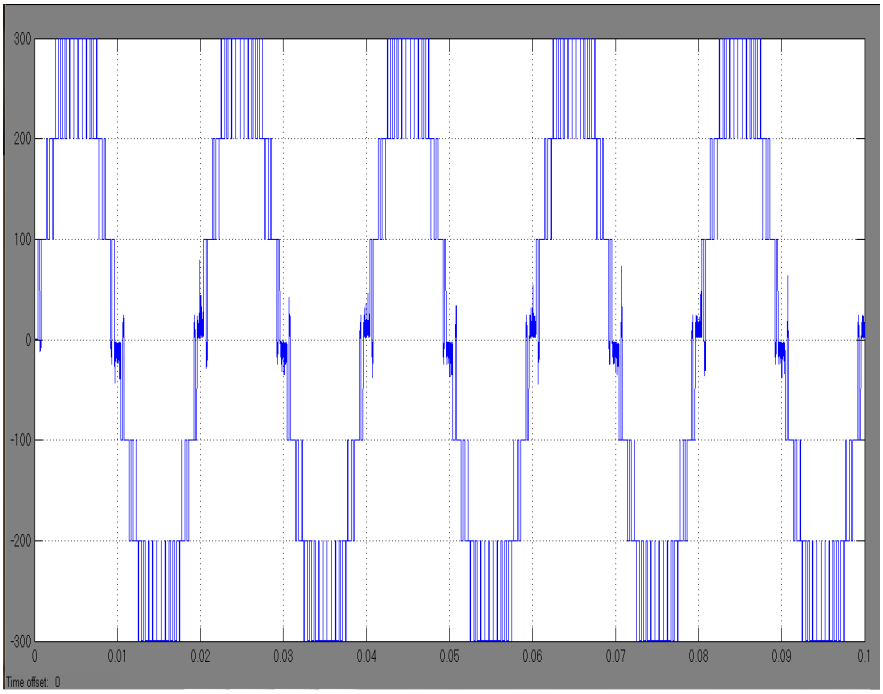

Figure 7. Output voltage of proposed inverter with RL-load

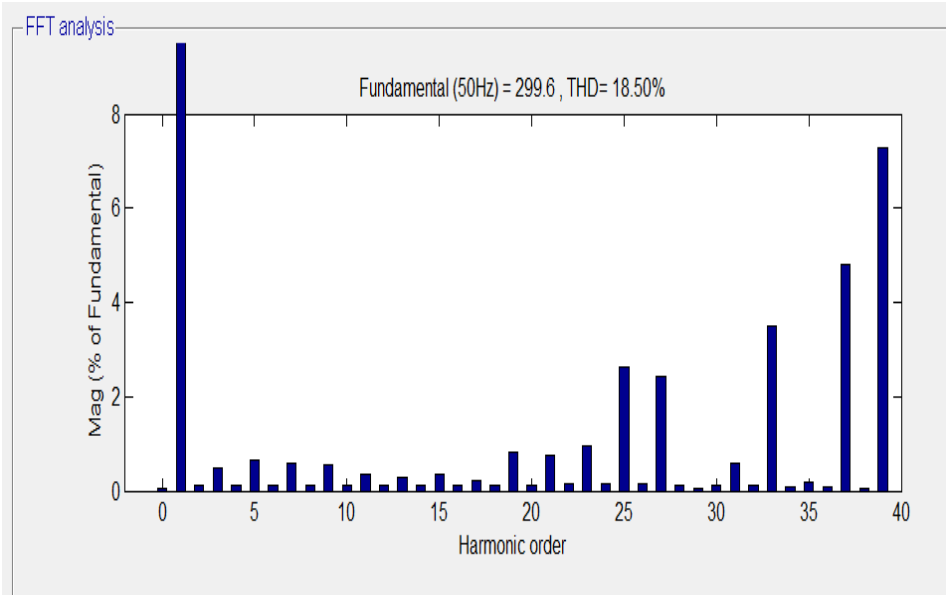

Figure 8. Harmonic spectrum of output voltage of the proposed inverter with RL-load

3.3. Proposed Circuit With Induction Motor

The proposed circuit consist of induction motor load in an output side of a simulation circuit. The simulation circuit is shown in a below figure 9.

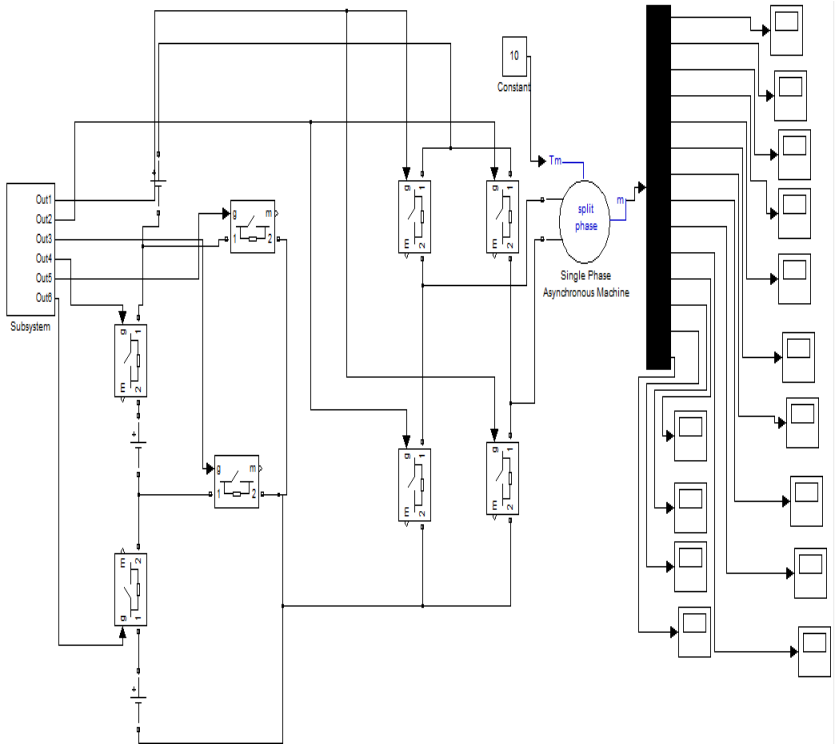

Figure 9. Simulation circuit for a cascaded H-bridge MLI fed with induction motor load.

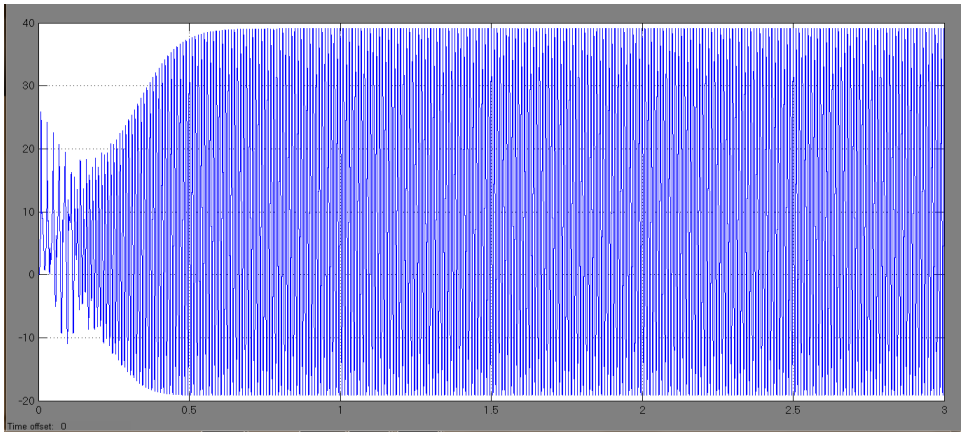

Figure 10. Speed of motor

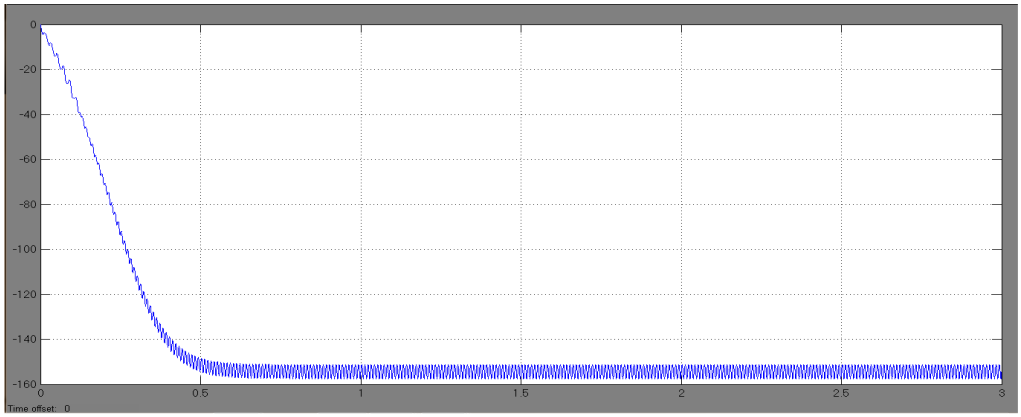

Figure 11. Torque produced by a motor

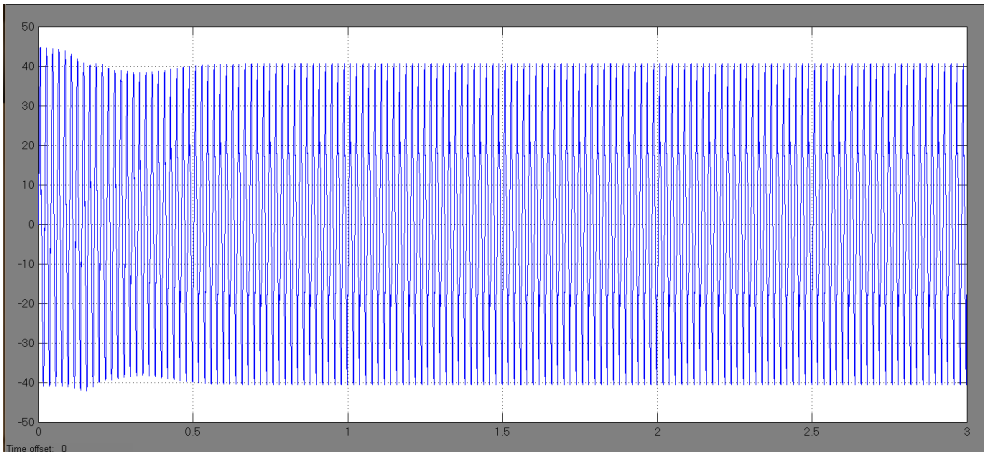

Figure 12. Main winding current of a motor

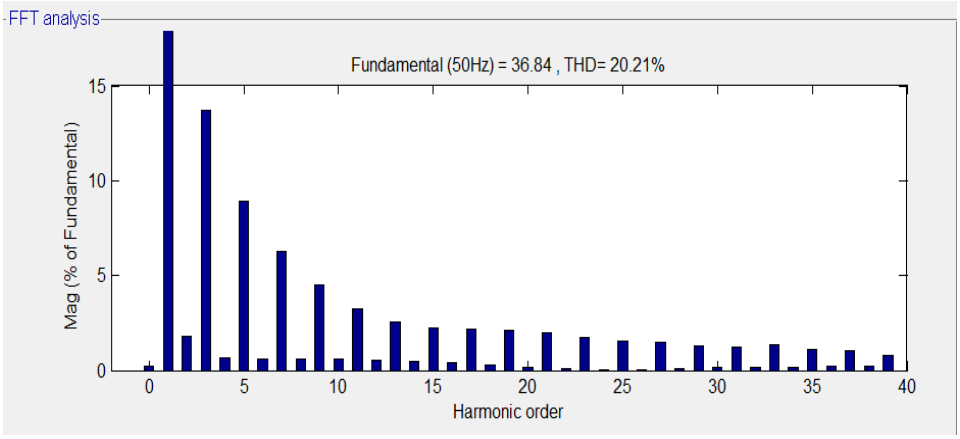

Figure 13. Harmonic spectrum of output voltage of the proposed inverter with induction motor load

Table 2. %THD value for different loads.

Single phase proposed inverter	**R-load**	**RL-load**	**Induction motor**
%THD	18.10	18.50	20.21

Table 3. V_{rms} value for different loads.

Single phase proposed inverter	**R-load**	**RL-load**	**Induction motor**
V_{rms}	212	211	220.6

4. CONCLUSIONS

In this paper the simulation results of single phase seven level cascaded multilevel inverter with R, RL and Induction Motor load are analysed by using MATLAB/SIMULINK. The output quantities like phase voltage, THD spectrum for a various load are obtained. The torque-speed characteristics of induction motor are also obtained. From Table 2 and 3 the cascaded multilevel inverter with R-load gives less %THD and it perform better than RL load and induction motor load. Depends upon the need of load we can use this cascaded multilevel inverter for various applications.

REFERENCES

[1] Holmes, D. G. and Brendan, P. M. (2001) "Opportunities for Harmonic Cancellation with Carrier Based PWM for two level and Multilevel Cascaded Inverters", *IEEE Trans. Ind. Appl.*, Vo1. 37, No. 2, pp. 574-582.

[2] Rodriguez, J., Lai, J. S., and Peng, F. Z., (2002) "Multilevel inverters:A survey of toplogies, controls and applications," *IEEE Trans.Ind. Electron.,* Vol. 49, No. 4, pp. 724–738.

[3] Y. Li, D. M. Vilathgamuwa, and P. C. Loh,(2004) ―Design, analysis, and real time testing of a controller for multi bus micro grid system", *IEEE Trans. Power Electronics*, vol. 19, no. 5, pp. 1195-1204.

[4] R. M. Tallam, R. Naik, and T. A. Nondahl,(2005) "A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Trans.Ind. Appl.*, vol. 41, no. 6, pp. 1734–1743.

[5] Leppanen, V. M. and Luomi, M.,(2006) "Observer Using Low-frequency Injection for Sensor less Induction Motor Control-Parameter Sensitivity Analysis", *IEEE Trans. Ind. Appl.*, Vol. 53, No.1,pp. 216-224.

[6] B.P.McGrath, D.G.Holmes and T.Meynard,(2006) "Reduced PWM harmonic distortion for multilevel inverter operating over a wide modulation range", *IEEE Trans. on Power Electron.,* Vol. 21, pp. 941–949.

[7] Rodriguez, J., Bernet, S., Pontt, J. O. and Kouro,S. (2007) "Multilevel Voltage Source Converter Topologies for Industrial Medium VoltageDrives", *IEEE Trans. Ind. Electron.,* Vol. 54, No. 6, pp. 290-294.

[8] D. Zhong, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, (2009) "DC-AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications", *IEEE Trans. Ind. Appl.*, vol. 45,no. 3, pp. 963–970.

[9] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau,(2010) "Survey on fault operation on multilevel inverters", *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207–2218.

[10] M. Malinowski, K. Gopakumar, J. Rodriquez, and M. Perez,(2010) "A survey on cascaded multilevel inverters", *IEEE Trans. Ind. Electron.*, vol. 57, no. 7,pp. 2197–2206.

[11] Sepahvand, H., Liao, J., Ferdowsi, M.(2011)"Investigation on capacitor voltage regulation in cascaded H-bridge multilevel converters with fundamental frequency switching", *IEEE Trans. Ind. Electron.,*vol.58, no.11, pp. 5102–5111.

[12] Ehsan Najafi and Abdul Halim Mohamed Yatim, (2012)"Design and Implementation of a New Multilevel Inverter Topology", *IEEE Trans. Ind. Electron.*, vol. 59, no. 11.

[13] C.R. Balamurugan, S. P. Natarajan and R.Bensraj, (2012)"performance and Evaluation of Three Phase Bridge Module Type Diode Clamped Multilevel Inverter", *International Journal of Engineering Trends and Technology,* Vol.3, No.3, pp.380-389.

[14] Saipadhma.S, Sangeetha.S and Kannabiran.A, (2013)" Comparison of Modulation Techniques for Cascaded and Reverse Voltage Multilevel Inverter Topologies", *International Journal of Advanced Trends in Computer Science and Engineering*, Vol.2, No.2, pp . 261- 266.

[15] Srinivas Reddy Chalamalla and S.Tara Kalyani,(2013) "Analysis of IM Fed by Multi-carrier SPWM and Low Switching Frequency Mixed CMLI", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,*vol.2,No.12,pp. 6295-6302.