APPLICATIONS OF FLOATING-GATE MOSFET IN THE DESIGN OF INVERTER AND RING OSCILLATOR

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ABSTRACT

This paper presents the application of floating-gate MOSFET (FGMOS) in the design of low voltage and high speed digital circuits wherein threshold voltage tunability of FGMOS has been exploited to enhance the performance of inverter in terms of various parameters like switching threshold voltage, noise margins, propagation delay and energy delay product. It has been observed that by varying the bias voltage in FGMOS, the voltage transfer characteristics can be altered that result in lowering of switching threshold voltage, increased noise margins, reduced propagation delay and less energy delay product as compared to the standard CMOS inverter. This paper also demonstrates the design of ring oscillator using FGMOS and it has been found that FGMOS based ring oscillator exhibits higher frequency of oscillation as compared to its CMOS counterpart. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 μm CMOS technology with a supply voltage of 1 V.

KEYWORDS

Floating-gate MOSFET, inverter, voltage transfer characteristics, propagation delay, energy delay product, ring oscillator

1. INTRODUCTION

The design of digital integrated circuits with very low power consumption and without much degradation in speed has always been the focal point of researchers particularly in sub-micron regime [1-3]. Since there is always a trade-off between power dissipation and time delay, therefore, reducing the power dissipation and still maintaining the appreciable performance in terms of operating speed is much desirable. With the immense demand of portable and battery driven applications, there is a need for new and alternative circuit design techniques to implement high performance and low power digital circuits. Further, with reducing feature size of devices, the lowering of operating supply voltage is obvious but at the expense of speed. Hence, for optimum performance of digital circuits, alternative design techniques should be explored [4-6].

CMOS inverter forms a basic building block of digital sub-circuits in mixed mode circuits with limitation of high switching threshold voltage resulting in degraded performance. Floating-gate MOSFET (FGMOS) has been widely used in the design of low voltage analog and digital circuits due to its unique characteristic of threshold voltage tuning with a bias voltage, thus imparting enhancement in performance. In this paper, we have employed floating-gate MOSFET (FGMOS) to design an inverter which has been further used to implement a ring oscillator. The paper has been divided in various sections briefly introducing FGMOS, its application in the design of inverter and ring oscillator. The performance of the designed circuits has been found to be enhanced vis-à-vis their conventional CMOS versions. The workability of these circuits has been

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verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

2. FLOATING-GATE MOS TRANSISTOR

The Floating-Gate MOS transistor (FGMOS) is basically a modified form of simple MOSFET where extra capacitances have been introduced between the conventional gate and the multi-input signal gates. By applying a bias voltage on one of the input gates, the threshold voltage of FGMOS can be reduced. A number of secondary gates or input terminals are deposited above the floating-gate (FG) which are electrically isolated from it but capacitively connected to it. Since FG is completely surrounded by highly resistive material, so for dc operation, FG acts as floating node. Programming of the FGMOS introduces a charge on its floating-gate that shifts the threshold voltage and thus, provides a control over the device functionality [7-10]. The equivalent schematic for an N-input and n-channel FGMOS is shown in Fig. 1 [11].

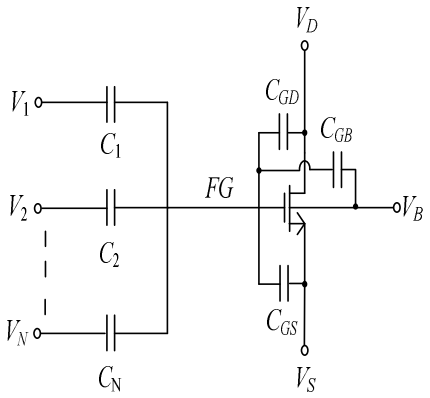


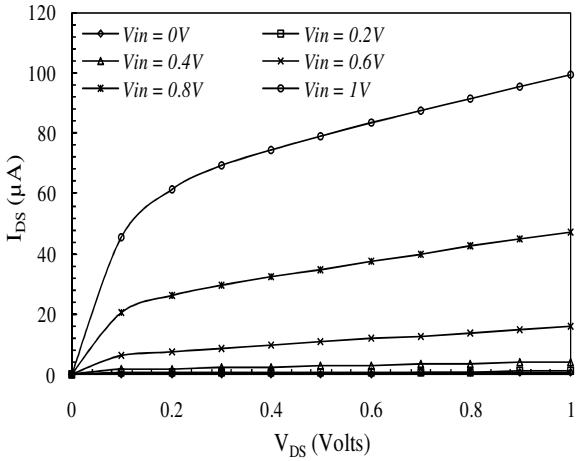
Figure 1. Floating-gate MOSFET

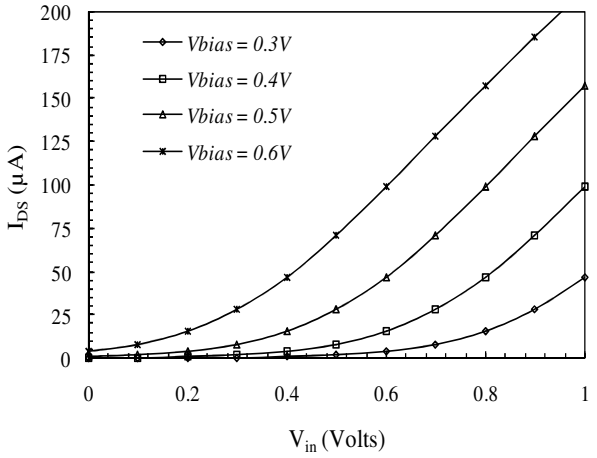
In a two-input n-channel FGMOS, input voltage (V_{in}) is applied through C_1 and bias voltage (V_{bias}) is applied through C_2 which provides tunability to the conventional threshold voltage (V_T) of the FGMOS and V_T adjusts to a new value $V_{T,eff}$ given as [12]:

$$V_{T,eff} = \frac{V_T - V_{bias} k_2}{k_1} \tag{1}$$

where $k_1 = \frac{C_1}{C_T}$ and $k_2 = \frac{C_2}{C_T}$ and C_1 and C_2 are the capacitances between floating-gate and control gates and $C_T = C_1 + C_2 + C_{GS} + C_{GD} + C_{GB}$. We observe that $V_{T,eff}$ will be less than V_T if we select $V_{bias} > V_T$ and $k_2 > k_1$, implying $C_2 > C_1$. Thus, in FGMOS we can select $V_{T,eff}$ lower than normal V_T.

Now, by selecting *W/L* of FGMOS as 1.3µm/0.13µm and with supply voltage of 1V, the drain and transfer characteristics are shown in Figs. 2 and 3 respectively.





It has been observed that as we increase V_{bias} from 0.3V to 0.6V, effective threshold voltage ($V_{T,eff}$) of n-channel FGMOS decreases from 0.8V to 0.2V at a reference drain current of 20 µA. Similarly, the drain and transfer characteristics for p-channel FGMOS show bias dependent behaviour. Thus, the performance of n-channel and p-channel FGMOS can be varied by optimum selection of their respective V_{bias} and making FGMOS based digital circuits suitable for low voltage and low power applications.

3. FGMOS INVERTER

The architecture of the FGMOS inverter has been obtained from the conventional CMOS inverter as shown in Fig. 4 [13]. The bias voltages V_{bp} and V_{bn} provide tunability to the threshold voltages of M1 and M2 respectively. It is, therefore, expected that by varying the bias voltages, the threshold voltage of the FGMOS inverter can be changed.

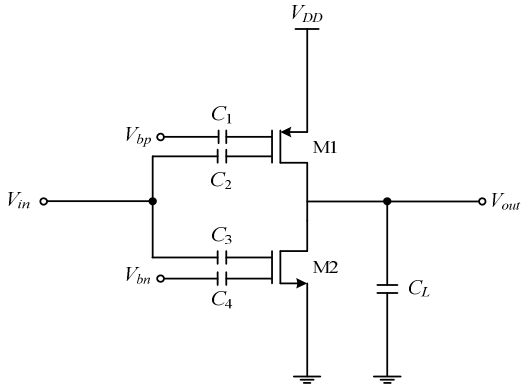


Figure 4. FGMOS inverter

The performance of FGMOS inverter can be characterized through its voltage transfer characteristics (VTC) which is a plot of V_{out} as a function of V_{in}. From these characteristics we can calculate parameters like switching threshold voltage and noise margins to ascertain the dc performance of these circuits. The switching threshold voltage (V_S) is defined as the input voltage that gives an identical output voltage and it can be obtained from the intersection of the VTC curve and the plot of $V_{out} = V_{in}$ [13, 14]. The voltage noise margins can be obtained as $NM_H = V_{OH} - V_S$ and $NM_L = V_S - V_{OL}$, where V_{OH} and V_{OL} are logic-high and logic-low output voltages of inverter respectively. Since noise margins NM_H and NM_L account for the sensitivity of a gate to noise, therefore large value of this parameter is desired that makes the gate less sensitive to noisy environment [15].

The switching threshold voltage for FGMOS inverter is given by [14]:

$$V_S = \frac{V_{DD} - \left|\frac{V_{Tp} - V_{bp}k_2}{k_1}\right| + \sqrt{\frac{\beta_n}{\beta_p}}\left(\frac{V_{Tn} - V_{bn}k_2}{k_1}\right)}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (2)$$

where $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$ and $\beta_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$ are transconductance parameters of n and p-channel FGMOS.

Now, the circuit of FGMOS inverter has been simulated to obtain the voltage transfer characteristics (VTC) at different values of V_{bp} and V_{bn} by selecting *W/L* of M1 as 26 µm/0.13 µm and M2 as 13 µm/0.13 µm with a supply voltage of 1 V as shown in Figs. 5 and 6 respectively.

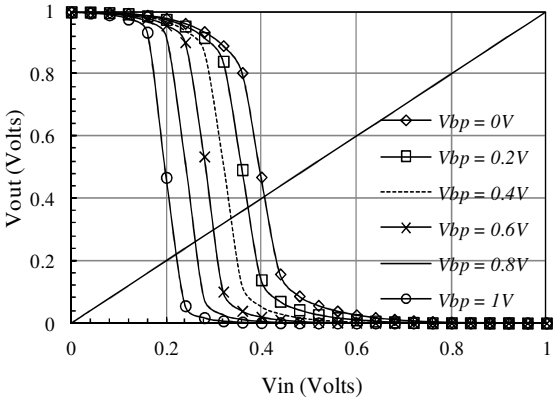


Figure 5. VTC of FGMOS inverter at different V_{bp}

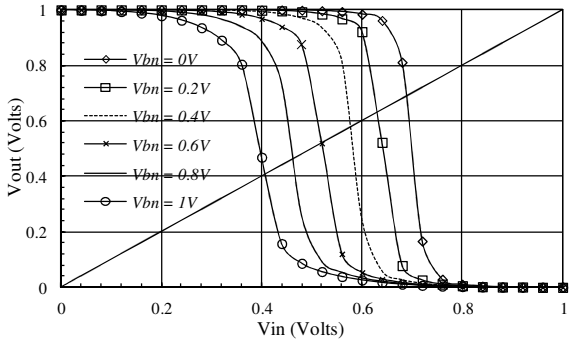


Figure 6. VTC of FGMOS inverter at different V_{bn}

From Figs. 5 and 6, the calculated values of the switching threshold voltage (V_S) and noise margins NM_H and NM_L at different values of V_{bp} and V_{bn} are given in table 1.

Table 1. Noise margins at different V_{bp} and V_{bn}

V_{bn} = 1 V fixed				V_{bp} = 0 V fixed			
V_{bp} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)	V_{bn} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)
0	0.40	0.60	0.40	0	0.68	0.32	0.68
0.2	0.37	0.63	0.37	0.2	0.63	0.37	0.63
0.4	0.33	0.67	0.33	0.4	0.57	0.43	0.57
0.6	0.29	0.71	0.29	0.6	0.52	0.48	0.52
0.8	0.25	0.75	0.25	0.8	0.46	0.54	0.46
1	0.21	0.79	0.21	1	0.40	0.60	0.40

As observed in table 1, when bias voltage of p-channel FGMOS (V_{bp}) is varied from 0 V to 1 V at constant bias voltage of n-channel FGMOS (V_{bn} = 1V), the switching threshold voltage (V_S) and low noise margin (NM_L) of FGMOS inverter decreases from 0.40 V to 0.21 V but high noise

margin (NM_H) increases from 0.60 V to 0.79 V. Similarly, when bias voltage of n-channel FGMOS (V_{bn}) is increased from 0 V to 1 V, while keeping V_{bp} fixed at 0 V, NM_L decreases from 0.68 V to 0.40 V. Now, in the circuit of FGMOS inverter, M2 (n-channel) determines NM_L and M1 (p-channel) determines NM_H and both noise margins are desired to be high for better noise immunity. From table 1, we observe that NM_H and NM_L are maximum when V_{bp} = 0 V & V_{bn} = 1 V which is the condition of low voltage operation for FGMOS because for V_{bp} = 0 V & V_{bn} = 1 V, M1 and M2 exhibits minimum value of threshold voltage. Therefore, better noise margins can be optimized by appropriate selection of V_{bp} and V_{bn} at 0V and 1V respectively.

The transient behaviour of the FGMOS inverter can be characterized by propagation delay (t_p) which is defined as the average of the time delay from low-to-high transition (t_{plh}) and from high-to-low transition (t_{phl}) of the input and output waveforms in an inverter. It specifies the operating speed and is given as [15, 16]:

$$t_p = \frac{(t_{plh} + t_{phl})}{2} \tag{3}$$

The propagation delay for FGMOS inverter can be given as [14]:

$$t_p = 0.35C_L\left\{\left[\beta_n\left(V_{DD} - \frac{(V_{Tn} - V_{bn}k_2)}{k_1}\right)\right]^{-1} + \left[\beta_p\left(V_{DD} - \frac{(V_{Tp} - V_{bp}k_2)}{k_1}\right)\right]^{-1}\right\} \tag{4}$$

Since t_p depends on threshold voltage of n and p-channel MOSFETs, therefore it is expected that it can be optimized using FGMOS where threshold voltage tunability is feasible [12].

The transient characteristics of FGMOS inverter at different values of V_{bp} and V_{bn} are shown in Figs. 7 and 8 respectively.

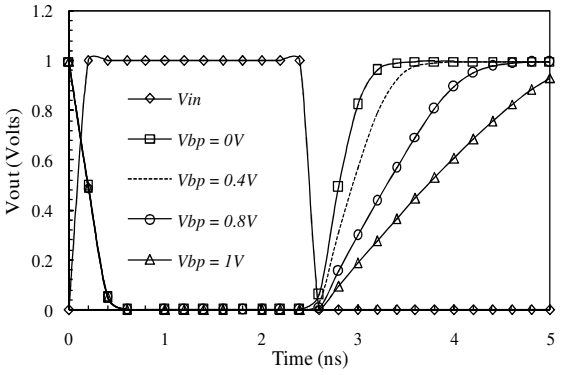
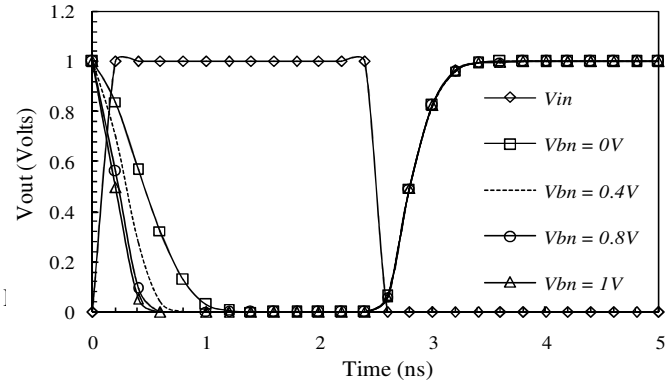


Figure 7. Transient response of FGMOS inverter at different V_{bp}



It is seen that the pulse response of FGMOS inverter can be varied with bias voltage resulting in different values of propagation delay as shown in Fig. 9.

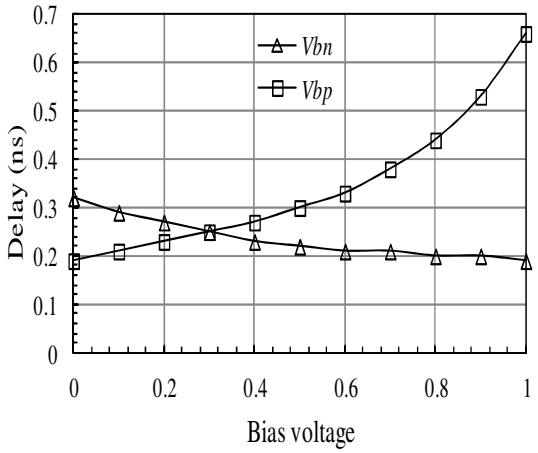


Figure 9. Propagation delay at different bias voltage

It has been observed in Fig. 9 that if the bias voltage of p-channel FGMOS is increased from 0V to 1V while keeping bias voltage of n-channel FGMOS fixed at 1 V, the propagation delay increases from 0.19 ns to 0.66 ns. Similarly, if bias voltage of n-channel FGMOS is increased from 0 V to 1 V while keeping bias voltage of p-channel FGMOS fixed at 0 V, the propagation delay decreases from 0.32 ns to 0.19 ns. Therefore, the appropriate selection of bias voltages of n and p-channel FGMOS at 1V and 0V respectively decreases the propagation delay of FGMOS inverter, thus enhancing the operating speed.

Now, the comparative transient characteristics of CMOS and FGMOS inverters have been obtained by selecting $V_{bp} = 0$ V and $V_{bn} = 1$ V as shown in Fig. 10.

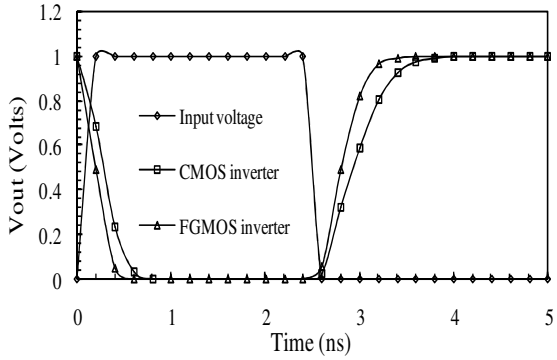


Figure 10. Comparative transient characteristics of CMOS and FGMOS inverters

From these results, it has been observed that FGMOS based inverter has less propagation delay (0.2 ns) as compared to CMOS inverter which has the propagation delay of 0.4 ns, implying that FGMOS based inverter exhibits better switching response and has high operating speed.

Since, the energy delay product represents the trade-off between power dissipation and the speed, implying the operation of digital circuits at low power would result in loss of speed. Therefore, lower value of energy delay product is required for circuits suitable for operation with low operating voltage and low power consumption without much loss in operating speed. Now, the values of propagation delay obtained from the transient analysis of CMOS and FGMOS based inverters has been used to calculate the energy delay product (EDP) at different values of V_{DD} as shown in Fig. 11.

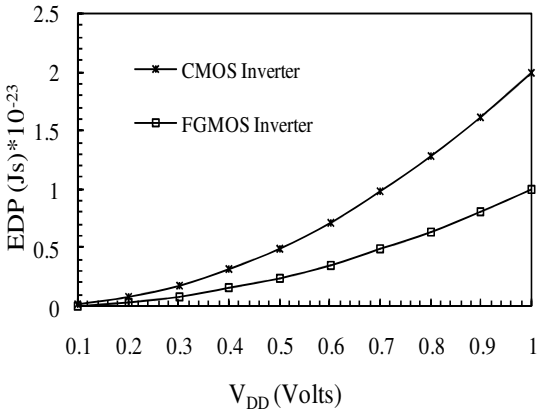


Figure 11. Comparative EDPs of CMOS and FGMOS inverters

The results obtained from Fig. 11 show that EDP is a function of supply voltage and for V_{DD}=1V, FGMOS inverter has EDP of 1×10^{-23} Js where as the value of EDP for CMOS inverter is 2×10^{-23} Js. Therefore, FGMOS inverter shows better performance as compared to CMOS due to lower value of energy delay product, thus posing as an alternative design technique for low voltage and high speed digital circuits.

4. RING OSCILLATOR

Since FGMOS inverter exhibits better response than its CMOS counterpart in terms of speed, noise immunity and power dissipation, therefore it has been further employed to implement a ring oscillator which is often used in the information, communication and sensor technology for frequency translation and channel selection [17-19].

A ring oscillator based on FGMOS is shown in Fig. 12 which consists of a cascade of three inverters and the frequency of oscillation is given by [20]:

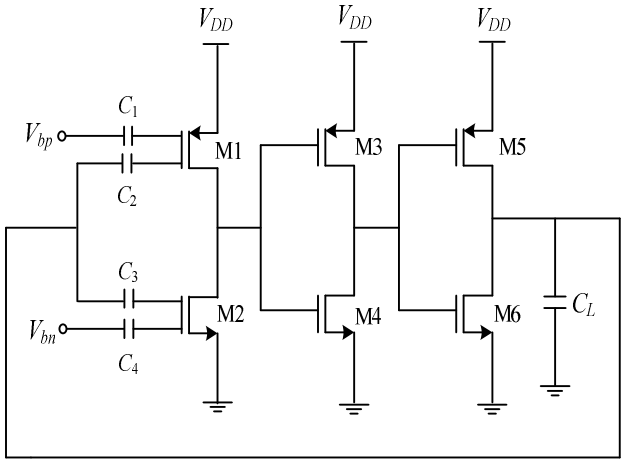


Figure 12. FGMOS based ring oscillator

$$f_o = \frac{1}{6\,(t_{phl} + t_{plh})} \tag{5}$$

where t_{phl} and t_{plh} are the propagation delay for high-to-low and low-to-high transitions respectively in an inverter which are given as under:

$$t_{phl} = \frac{C_L k_1 (k_1 V_{DD} + V_{Tn} - V_{bn} k_2)}{\beta_n (k_1 V_{DD} - V_{Tn} + V_{bn} k_2)^2} \tag{6}$$

$$t_{plh} = \frac{C_L k_1 \{k_1 V_{DD} + 3(V_{Tp} - V_{bp} k_2)\}}{\beta_p (k_1 V_{DD} + V_{Tp} - V_{bp} k_2)^2} \tag{7}$$

$$t_{phl} + t_{plh} = C_L k_1 \left(\frac{k_1 V_{DD} + V_{Tn} - V_{bn} k_2}{\beta_n (k_1 V_{DD} - V_{Tn} + V_{bn} k_2)^2} + \frac{k_1 V_{DD} + 3(V_{Tp} - V_{bp} k_2)}{\beta_p (k_1 V_{DD} + V_{Tp} - V_{bp} k_2)^2} \right) \tag{8}$$

From Eq. 8, we see that propagation delay decreases with increase in V_{bn} and decrease in V_{bp}. Therefore, increasing bias voltage of n-channel FGMOS while keeping bias voltage of p-channel FGMOS at zero volt will lead to small propagation delay and hence, enhanced frequency of oscillation. Now, the circuit of FGMOS ring oscillator has been simulated at different values of V_{bn} while keeping V_{bp} fixed at 0 V by selecting *W/L* of M1, M3 and M5 as 26µm/0.13µm and M2, M4 and M6 as 13µm/0.13µm with the supply voltage of 1 V. The simulation results are shown in Fig. 13.

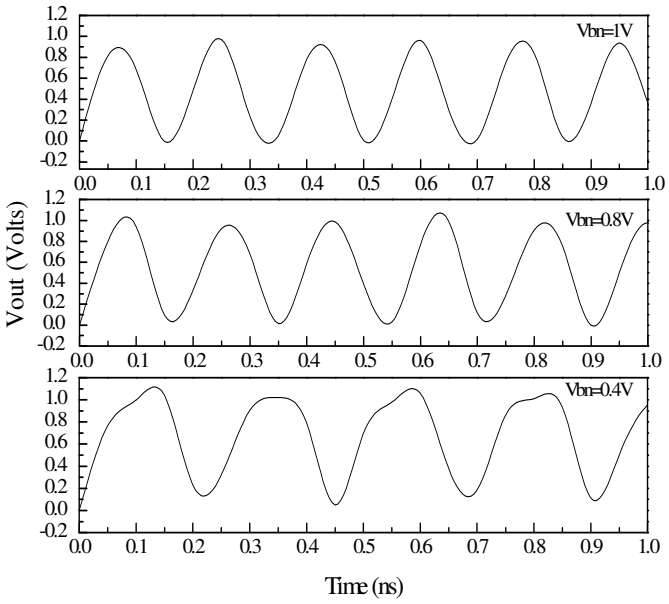


Figure 13. Oscillations of FGMOS based ring oscillator at different V_{bn}

From the above results we have observed that the frequency of oscillation increases with increase in bias voltage (V_{bn}) as shown in table 2.

Table 2. Variation of f_o with V_{bn}

V_{bn} (V)	f_o (GHz)
0.2	4
0.4	4.5
0.6	5.2
0.8	5.9
1	6.7

The comparative performance of CMOS and FGMOS based three stage ring oscillator has been obtained by selecting V_{bp} = 0 V and V_{bn} =1 V and is shown in Fig. 14. It has been observed that frequency of oscillations in FGMOS ring oscillator is 6.7 GHz while for CMOS ring oscillator it is 5 GHz.

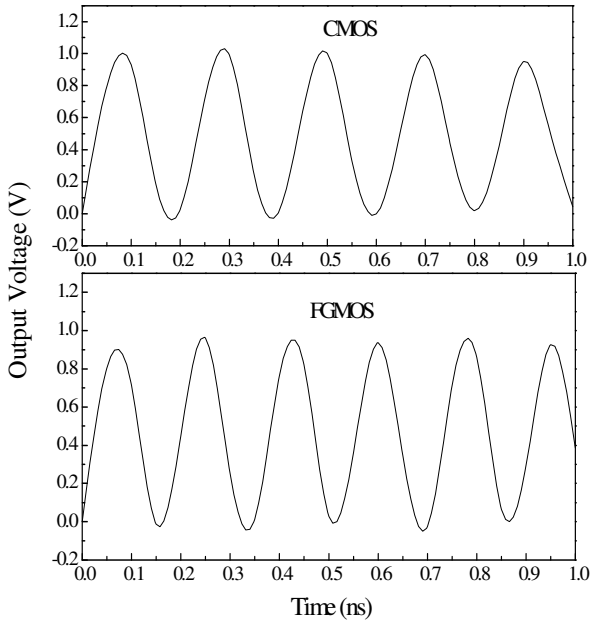


Figure 14. Oscillations of CMOS and FGMOS based ring oscillators

The number of inverter stages in ring oscillator may be increased for multiphase outputs but at the expense of reduced operating speed, high power dissipation and large chip area [20]. The comparative frequency of oscillations in ring oscillator using CMOS and FGMOS with different stages is given in table 3

No. of stages	**CMOS**	**FGMOS**
	f_o **(GHz)**	f_o **(GHz)**
3	5	6.7
5	3.3	3.8
7	2.5	2.8
9	2	2.1

Table 3. Comparative oscillation frequency of multistage ring oscillator

From the above results, we observe that with increase in the number of inverter stages in the structure of ring oscillator, the frequency of oscillation decreases due to increased propagation delay.

5. CONCLUSIONS

In this paper, we have studied the effect of threshold voltage tunability in FGMOS for enhancing the performance of inverter and ring oscillator. It has been found that by varying the bias voltage of FGMOS, the voltage transfer characteristics of inverter can be suitably altered resulting in decreased switching threshold voltage, increased noise margins, reduced propagation delay and energy delay product as compared to its CMOS version. Further, it has been observed that the oscillation frequency of ring oscillator depends on the propagation delay of inverter stages and FGMOS based ring oscillator exhibits higher frequency of oscillation as compared to CMOS ring oscillator.

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