ENERGY-EFFICIENT LOW DROPOUT REGULATOR WITH SWITCHING MECHANISM AND COURSE REGULATOR FOR INTERNET OF THINGS (IoT) DEVICES

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ABSTRACT

The proposed work presents an Energy-efficient, low dropout (LDO) regulator with switching mechanism reduces the energy consumption of IoT devices when the sensors are in idle time. Based on the analysis of IoT devices and sensors, modern power management designs for IoT demands for fully integrated solutions to decrease power consumption while maintaining the quick transient response to signal variations. LDO voltage regulators, as power management devices should adjust to modern technological and industrial trends. To increase the current capability with a minimum standby quiescent current under small-signal operation, the proposed work has a switching circuit acting as an ON and OFF switch. To reduce the dropout a course regulator and loop filter is added and circuit is enhanced for maximum reduced dropout. As a result, the efficiency gets increased.

KEYWORDS

Internet of Things, Low Dropout Regulators, Error Amplifier

1. INTRODUCTION

Internet-of-things (IoT) consists large amount of smart devices that are being connected using internet as backbone. The power supply for these products is often taken for granted. However, predicting from recent experience, it’s evident that the power supply for IoT products is a major factor for its success and reliability. Most of the IoT devices solely operate for a very short amount of time and sleep or standby for a longer duration. This very low duty cycle feature makes the ultra-low stand-by power a critical specification for the IoT devices to withstand the battery life and charge cycle [1]. Various functional integration in power management which has embedded circuits is just the way of extending the battery life of IoT devices. A fortuitous understanding observed from the current designs that the low-dropout (LDO) regulator can help to achieve demanding power supply needs of such devices [2]. Whether the power-supply design operates from the ac line or batteries, the LDO is the primitive solution that are simple low-priced method to improve an output voltage which is mechanized from an increased voltage input.

Based on a novel approach [3], DC-DC converter accomplish high efficiency but it suffers from the slow response and extra cost due to off-chip components. Contrarily, LDO regulator has various advantages such as low-voltage analog, mixed-signal, smaller die area, minimal external passive components, higher accuracy, fast transient response and lower noise [4]. The power
efficiency of the DC-DC converters at light load current becomes demanding specifically when the System-on-Chip’s (SoCs) operate in the sleep mode. This is important for portable IoT devices where the device is to be sleep mode. By considering these tradeoffs this paper introduces a power efficient design with switching mechanism for LDO so that the dropout for LDO can be minimized to the maximum.

2. RELATED WORK

The conventional circuit diagram of LDO with battery supply which uses a PNP transistor as the series pass device consists of the following primary components 1) Voltage Reference or Bandgap 2) Error Amplifier 3) A Pass element and 4) Feedback Network[5]. As shown in the following LDO circuit, the input is applied to the pass element. This pass component operates in definite region to drop input voltage all the way down to the extent required as output voltage. The ensuing desired output voltage is perceived by error amplifier. This is correlated with reference voltage. The error amplifier is used to drive the gate of the pass element to operating point to ensure correct output voltage based on the fixed voltage reference (VREF). The error amplifier modulates pass element to maintain constant output voltage when operating current or input voltage changes.

An LDO is a linear feedback voltage regulator that has a low dropout or overhead voltage. The overhead voltage represents the difference between the input and output voltages and the lowest value that can occur before the closed-loop regulation stops working. Therefore LDO efficiency [5] is calculated by getting the ratio of output voltage (V_{OUT}) and input voltage (V_{IN}). While considering regulator operating current the LDO’s efficiency can be expanded using the full formula,

\[
\text{Efficiency} = \frac{V_{OUT} \times I_{OUT}}{(V_{IN} \times I_{GND})} \times 100 \tag{1}
\]

Many designs are proposed for LDO in the aspects of noise reduction, stability and efficiency. A low-power bandgap voltage reference (BGR) is designed to supply a voltage reference for a low-voltage LDO. For process technology lower than m, the supply voltage for circuit has gone down to 1.20V. The decreasing transistor size has also encouraged the trend of system integration into a full-chip which is called Silicon on Chip (SoC). The lower power consumption requirement is therefore becoming more critical to reduce the heat and also extends the battery life. Low-power Bandgap design [6] proposed for LDO to maximize the battery life to decrease the voltage reference (V_{REF}) value. Though the design is efficient to provide low V_{REF}, it forgets to address variation dependency on temperature.
The LDO regulator structure consists of an ERR AMP, a power transistor (PWR TR) and feedback resistors. The ERR AMP generates the error signal based on a comparison between the feedback signal from a resistive divided output voltage and the reference voltage. To supply a large output load current, the PWR TR is huge when compared with the other transistors; therefore, the parasitic capacitor \( C_p \) at the gate of the PWR TR is very large. Large gate capacitance of a PWR TR restricts the Slew Rate (SR). To enhance SR capacitor-less model[7] has been proposed. It proposes additional SR enhancement circuit which improves the feedback based on voltage-spike detection when the voltage changed at the output node.

In analog LDO designs [8]–[9], the control loop latency is reduced using a high-speed error amplifier. However, such amplifiers generally consume a large amount of power, and furthermore become less effective at supply voltage (VDD) less than 1V due to the limited headroom problem. Most linear regulators use an NPN transistor or N-type MOSFET for the series control element. The output voltage is monitored and compared to a fixed stable reference to develop a feedback control error signal. Power dissipation in the transistor is created by overhead voltage and load current. Heat and wasted power leads to undesired consequences over here. An LDO solves this problem by using a PNP transistor or P-type MOSFET as the series pass device is the now a current source or amplifier rather than an emitter (source) follower. This paper proposes an LDO design that concentrates on all primary components in all the aspects which helps in maximizing efficiency of LDO to the maximum level which in turn increases reliable power supply for IoT devices.

3. PROPOSED LDO ARCHITECTURE

Before explaining about the proposed LDO architecture, telemetry of IoT devices are taken into account. When collecting data from devices, there are two fundamental choices (1) Pull the data periodically (PULL) (2) Devices sending the data with no prompting (PUSH). Each device or the device's microcontroller has three device power modes active, idle and standby in addition to an optional, zero-watt, power-removed mode. These sensor devices already been provided with limited amount of power and hence by utilizing the periodic aspect of sensors, we can switch the hardware components to OFF state. This results in efficient power management at hardware level of sensors. In the power management block (PMB) of IoT, LDO plays a vital role that regulates an output voltage that is powered from a higher voltage input. The proposed model consists of 1) course regulator 2) switching circuit and 3) loop filter.

![Block Diagram of Proposed Architecture](image-url)
In LDO, reference voltage ($V_{REF}$) source is important to block both in analog and digital–analog mixed circuit. With the decrease in feature size, and considering the reliability of the device, the operating voltage of the circuit is also reduced. Meanwhile, with the rapidly increasing scale of integrated circuit chip, the power consumption of the circuit has limited source. The basic principle of bandgap voltage reference is that two quantities having opposite temperature coefficients of the voltage are added with legitimate weighting, and finally produced a zero temperature coefficient voltage. Using equation (2) $V_{REF}$ is calculated and output voltage ($V_{OUT}$) is estimated based on it.

$$V_{REF} = V_{BE1} + R_2I_2 = V_{BE1} + \frac{R_2}{R_1} \Delta V_{BE}$$

(2)

where $V_{REF}$, $R_1$ and $R_2$ are dependent on Temperature(t). And hence output voltage is determined using equation (3).

$$V_{OUT} = V_{REF} \left( \frac{R_2}{R_1} \right)$$

(3)

The process of the circuit is to reduce the given input to a desirable amount suitable for the particular IoT device or controller. It starts with a course regulator which reduces the amount of power given as input. Even though the circuit regulates heavy power supply, the output of this particular circuit has a lot of noise. Reducing the noise by using LDO with loop filter, gives noiseless and regulated power supply. The next circuit used is the switching circuit, which consists of P-MOSFET which acts like switch. Finally, the desired low-power output is obtained with reduced noise. The energy ($E$) and power ($P$) consumption of the circuit is estimated using the following formulae.

$$E = \int_0^t V(t).I(t)dt$$

(4)

$$P = \frac{1}{t} \int_0^t V(t).I(t)dt$$

(5)

And finally the overall efficiency of the LDO is obtained by substituting the values in equation(1). The estimation shows approximately 50% of the increase in efficiency by the proposed LDO design.
3.1. Course Regulator

The course regulator consists of a buck converter which steps down the voltage from the input to the output. It consists of two semiconductors and one storage element. It provides up to 90% efficiency and it does not consume more power. Even the smaller proportion of current flows through the controller in idle state is sufficient for it. The buck controller in the simulated results is tested with 12V supply and output obtained is nearly 6V. Units. Course regulator possess higher efficiency than LDO as it maintains its input and output power almost equal there by reduces voltage regulation loss as in the case of LDOs which will have power wastage in regulating switch but advantage of using LDO in to power devices lies in the fact that it will have good transient response with less ripple in the output thus we will have good line and load regulation with good transient response. Thus we combined both Switching regulator and LDO in our design. We used switch regulator as a coarse regulator and LDO as a fine regulator in order have higher efficiency by reducing initial power loss in converting input voltage to voltage nearer to our requirement then doing the fine regulation to feed the device.

3.2. Switching Regulator

Switch regulator reduces regulation loss by using reactive elements to reduce the power loss in conversion. In our design we use switching regulator as a coarse regulator to avoid the loss in using LDO to regulate voltage having higher difference between input and output.
the LDO will be in OFF state, by saving the power. While switching, energy overhead ($E_{OVERHEAD}$) is considered to estimate the saved energy ($E_{SAVED}$) due to switching.

$$E_{ACTIVE} = P_{ACTIVE}(t_{event} - t_1)$$  \hspace{1cm} (6)

Average power consumption for $P_{ACTIVE}$ to $P_{OFF}$ is

$$E_{SAVED} = (t_{event} - t_1) \cdot P_{ACTIVE} \cdot \left( \frac{P_{ACTIVE} + P_{OFF}}{2} \right) + (t_{event} - t_1 - T_{down}) \cdot P_{OFF}$$  \hspace{1cm} (7)

In equation (7) energy saved is manipulated when the switching operation happens.

$$E_{OVERHEAD} = \frac{T_{up}(P_{ACTIVE} + P_{OFF})}{2}$$  \hspace{1cm} (8)

Switching to OFF state is beneficial if $E_{OVERHEAD} < E_{SAVED}$. From the simulated results, shown in table 1 switching is highly beneficial when long running IoT devices and also devices with periodic sensors where the device is in idle state for more time. As our application involves IOT data application, we can switch off our power module at regular interval to avoid idle state power loss. It will increase our efficiency to further extent. PMOS switching is used as it will helps in switching with minimal overdrive.

Figure 6. State Transition for Power

Figure 7. Secondary Switching Circuit
3.3. LDO and smoothing loop filter

LDO sets the constant output by varying the voltage drop across MOSFET switch in series with the load to maintain the output irrespective of the changing load. Negative feedback is used to minimize the error in regulating the output irrespective of changing load. Loop filter is used to reduce ripples in the output by smoothening the output changes caused by the changing load.

![Figure 8. Circuit Diagram of Loop Filter](image)

A low-pass filter (LPF) has a resistor and capacitor, which is added to the LDO. This circuit plays a major role in reducing the noise thereby providing a more efficient output. Loop filter is used to smoothen the values. It enhances the work of LDO. Cut-off frequency of this filter is set between 1 and 500 Hz, therefore filtering all the noise coming from the bandgap.

4. ANALYSIS AND RESULTS

The proposed model is simulated using LTspice simulator. In Figure 9 states time vs energy for LDO with and without switching, shows the fluctuations in energy savings.

![Figure 9. Time Vs Energy comparison for LDO with switching mechanism](image)
In Figure 10 states time vs energy for LDO with and without course regulator which plays an important role in reducing energy dissipation, which implies on energy savings.

![Figure 10. Time Vs Energy comparison for LDO with course regulator](image)

4.1. Dropout Voltage

It is the minimum voltage needed in the regulator to maintain regulated voltage output or regulation. For example, if LDO regulator has 3.3V regulated output and it has 1V as dropout voltage then input voltage should be at least 4.3V to maintain regulation. The input to output differential voltage at which circuit stops to regulate against any further input voltage reductions. This occurs when input voltage reaches near to the output voltage. It is expressed in terms of ON-resistance as follows. Here the Io is obtained as an output current.

\[ V_{\text{dropout}} = Io \times R_{\text{ON}} \]  

The below figures 12 – 21 are the screenshots of various outputs obtained by providing 6V and 12V as source input by using LTSPICE simulator. The outputs have been compared with both switching and non – switching mechanisms. And it is evident from the below outputs, hence by implementing the switching mechanism dropout voltage is been greatly reduced in LDO.

![Figure 11. I/P energy of switching circuit for 6V](image)  
![Figure 12. O/P energy of switching circuit for 6v](image)
Figure 13. I/P energy of non-switching circuit for 6V

Figure 14. O/P energy of non-switching circuit for 6V

Figure 15. Input-output curve for source voltage of 12V

Figure 16. Input-output curve for source voltage of 6V

Figure 17. I/P energy of switching circuit for 12V

Figure 18. O/P energy of switching circuit for 12V

Figure 19. I/P energy of non-switching circuit for 12V

Figure 20. O/P energy of non-switching circuit for 12V
4.2. Efficiency

The LDO regulator efficiency is projected in equation (10).

\[
\text{Efficiency} = \frac{(Io*Vo)}{((Io+Iq)*Vi)}*100
\]

(10)

The dropout voltage and quiescent current is minimized to achieve higher efficiency. Moreover voltage reduction between input and output also should be minimized.

Table 1. Efficiency of Switching and Non-switching circuits.

<table>
<thead>
<tr>
<th></th>
<th>(V_s)</th>
<th>Input Energy[mJ]</th>
<th>Output Energy[mJ]</th>
<th>Efficiency %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Switching</td>
<td>6V</td>
<td>1.351</td>
<td>0.408</td>
<td>30</td>
</tr>
<tr>
<td>Switching</td>
<td>6V</td>
<td>1.188</td>
<td>0.473</td>
<td>39.8</td>
</tr>
<tr>
<td>Non-Switching</td>
<td>12V</td>
<td>2.822</td>
<td>0.448</td>
<td>15.87</td>
</tr>
<tr>
<td>Switching</td>
<td>12V</td>
<td>2.541</td>
<td>0.512</td>
<td>20.14</td>
</tr>
</tbody>
</table>

From the above table 1, it is clear that by using the switching circuit, the efficiency of the LDO gets increased there by reduces conversion loss between the input and output the value increases nearly 8 percent.

5. CONCLUSION

By using switching circuit we can dynamically reduce the energy loss during conversion thereby increasing the overall efficiency, especially for sending small loads. Meanwhile, superior load regulation is obtained by reducing the variation of the input voltage difference of the LDO’s error amplifier.

REFERENCES


AUTHORS

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