SOC-Based Sensor Mote Design

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ABSTRACT

In this paper, a development of sensor node for environment monitoring is described. The Reconfigurable System-On-chip (RSOC) technology is used to integrate the node's main components on Field-Programmable Gate Array (FPGA) chip. The main components required to support the environmental applications such as pixels sensor, reconfigurable processing core, and a tiny solar unit for recharging node's battery, are implemented on the node. The use of FPGA chips has made such nodes consume large power. Therefore, nodes are provided with tiny rechargeable unit to recharge the nodes' batteries. The nodes should be installed at well-setting environmental applications, where nodes are carefully distributed over the environmental applications field to be exposed to daylight, which will help recharge nodes' batteries. Applications such as border control and forest fire monitoring can use such nodes at their wireless sensor networks.

KEYWORDS

Wireless Sensor Network, FPGA, Hardware reconfigurations, Well-setting environmental applications

1. INTRODUCTION

Recent advances in wireless communications and electronics have enabled the development of wireless sensor networks that use low-cost, low-power, multifunctional sensor nodes. These tiny nodes design consist of sensing, computing, communication units, and some other application-dependent units such as power generators and location finding units [1-3]. Such networks offer economically viable solutions for applications that can be found in different settings such as industry, military, environment, health, etc. [4, 5]. Sensor nodes are generally designed and programmed to match the needs of the target applications before they are released to the field.

Many Wireless Sensor Networks (WSNs) are new and their requirements may not be fully anticipated during the sensor networks design and development stage. Remotely adding or modifying the design of sensor nodes to support new or modified software features required by target applications can be currently achieved using software reprogramming capability, which is supported with existing WSNs [6, 7, 8]. However, remote hardware reconfiguration capability could be very useful for some WSNs applications. To support this capability, sensor nodes will require using Field Programmable Gate array (FPGA) technology at their design. The WSNs nodes are not using FPGA yet in their design due to the large power consumption of this technology. However, the use of FPGA will provide nodes with important design features of flexibility and reconfigurable processing unit.

This research is to foster the development of new and novel wireless sensor node for next-generation WSNs infrastructure. The proposed sensor node will be unique in providing remote software reprogramming and hardware reconfiguration capabilities. We will use the term '***RR-node***' whenever a reference has been made to the proposed node's infrastructure. Using the proposed RR-node in next-generation WSNs will produce flexible infrastructures that will

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provide remote design modification even after the deployment of WSNs on the sensing field. In addition, the RR-node can be used for other application fields such as vehicle electronics, mobile phones, security systems, etc.

There are some design challenges associated with the RR-node development such as provide RR-node with remote hardware reconfiguration capability, reducing high power consumption due to the use of FPGA Technology in node design, develop a library for RR-node components, and developing WSN prototype to provide a proof-of-concept for using RR-nodes in supporting a real-world applications such as security surveillance, border control, forest fire monitoring, etc. In this paper, we will address some of these challenges and specifically using FPGA technology and pixels sensor in node design for monitoring applications. The developed of flexible FPGA-based node infrastructure will be important for advancing research in the area of WSNs remote sensing, development, and applications.

2.DESIGN CONCEPT

Some of the existing WSNs have the support for software reprogramming capability, where the software modifying on individual nodes can be achieved after the network has been deployed and initialized [9, 10]. However, the remote support for both software reprogramming and hardware reconfiguration capabilities has not been available in existing WSNs' nodes. Therefore, in this RR-node development project, the focus will be given only to the hardware reconfiguration since it is a new WSNs capability that has not been investigated thoroughly yet. The design and the development of the proposed RR-node instrument is new, novel, and crucial to explore the use and the impact of the RR-node on next-generation WSNs and applications, which require on-field system modifications. The development of the proposed RR-node will provide WSNs with sensor nodes that have a unique fully dynamically adaptable feature. This feature will provide nodes design with adjustable capability to their surrounding environment even after their deployment on the sensing field.

Supporting the proposed RR-node instrument with hardware reconfigurations capability will require the use of FPGA technology in nodes design. The existing WSNs nodes have no FPGA in their designs due to the main drawback of the FPGA, which is high power consumption. However, the effect of this problem can be reduced and may be eliminated by using modern FPGA chips that consume low power such as Spartan 3L, Actel gloo, etc. Also, the partial reconfiguration that supported in some FPGA design tools such as Xilinx ISE, can reduce the size of the design bit stream file that will support fast remote hardware reconfiguration with less power consumption.

In addition, the use of low-cost and tiny solar units in this project to recharge the RR-node batteries will elevate the drawback for the large power consumption of using FPGA in WSNs. Increasing the cost of the RR-node due to the use of solar unit with each node might not be acceptable in low-cost WSNs. Nevertheless, the RR-node increased cost can be acceptable for some other WSNs applications, which require high performance processing nodes and/or provide nodes' design adaptability to their surrounding applications. The environmental monitoring applications such as forest fire detection, homeland security, border control, etc., are some of the potential applications that could use the RR-nodes.

The existing nodes' wireless channel that used for WSNs routing will also be used to support the RR-node design with remote hardware reconfiguration capability. As most of the commercially available FPGA chips include a JTAG port to download the configuration file, the use of wireless JTAG unit will be used to provide RR-node design with hardware reconfiguration capability.

3.RR-NODE DEVELOPMENT

The main components of RR-node are the soft-core MIPS processor, pixel sensor interface, and the wireless JTAG unit controller that are designed using VHDL language and all integrated on a single Xilinx FPGA Spartan 3 chip. All other off-the-shelf nodes' components such as the pixels sensor, wireless transceiver, memory, battery unit, communications antenna, CPLD chip for JTAG controller, and the Xilinx FPGA chip are all integrated on a small PCB board to produce the prototype RR-node.

The MIPS processor used in RR-node design is a soft-core architecture which is designed to be optimized, flexible, and efficient for the need of the WSN application. The instructions set and the architecture of the soft-core MIPS processor can be optimized to the needs of the target WSNs applications through the use of hardware reconfiguration capability provided in the design RR-node through its wireless channel. The developed soft-core processor performance provides 10 MIPS, which is efficient to meet the processing needs most of the target applications [11, 12]. In addition, the soft core processor has a flexible design that supports remote hardware modification on the applications field. The processing core is small and can be integrated on the FPGA chip with other required RR-node components [Figure 1].

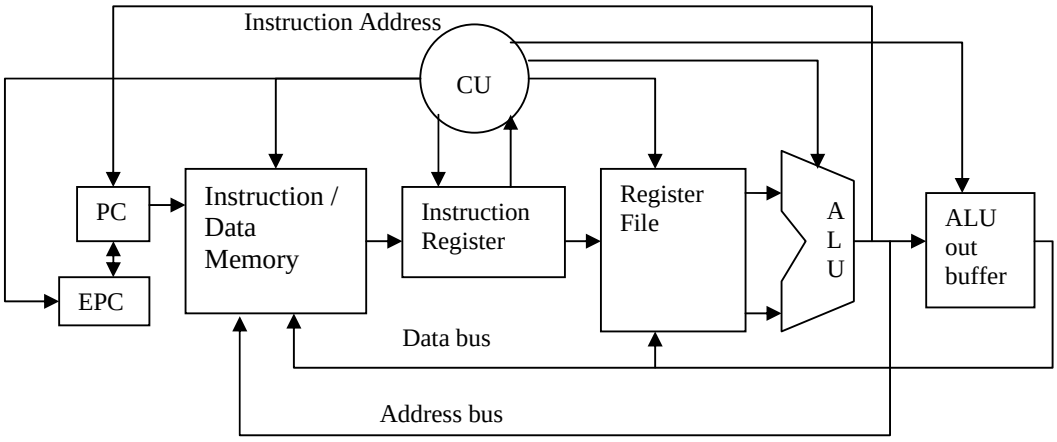

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Figure 1: Developed Soft Core Processor Architecture for RR- Node

To minimize the power consumption required to support the hardware reconfiguration of WSNs node, the size of the bit stream file for the reconfiguration component using partial reconfiguration approach and data compression provided by the FPGA design tools must be minimized. We have evaluated the hardware reconfiguration that performed to adjust the data path for the ALU and RF from 16-bit to 32-bit. The VHDL code for these two components was synthesized using Xilinx ISE design tools for Xilinx SPARTAN 3 chip. The default bit stream file size produced by the Xilinx ISE design tools for each of these components is 344,468 bytes. However, using the file compression option provided by Xilinx design tools, the bit stream file size for both components was reduced significantly as shown in Table 1.

The transfer time for the bit stream design files for the ALU and RF components produced to reconfigure the soft-core processor designed for Spartan device XA3S700A was found to be 6.1

and 35.5 seconds respectively. Clearly, the transfer time for the hardware reconfigurable components was large due to the use of slow transceiver that provides 64Kbit/sec.

This measurement was based on a design of a 32-bit ALU that can process 15 different operations and RF with 32 registers where each register has 32-bit. The design bit stream file for each component was produced using VHDL synthesizer of the Xilinx ISE design tools and transferred using a simple data packet frame format, which has 8-bit header and 8-bit trailer, 8-byte size for the hardware reconfiguration data transfer, and a CRC field. Such timing requirement for upgrading the processor design between 16 and 32-bit architecture is useful to evaluate the amount of time that required upgrading the soft-core processor. Such upgrading is important to support new application's features, which was not supported by processor when the RR-node deployed on the application field.

	16 bit, 16 register		32 bit, 32 register	
Component	ALU	RF	ALU	RF
SPARTAN 3A Device:XA3S700A	40KB	54KB	43KB	281KB

Table 1:
ALU and RF bit stream file size

The developed node has a CMOS pixels sensor to detect moving object appeared in the captured image, which can be used to support monitoring applications such as security surveillance. The design bit stream file of the pixels sensor interface was found to be 45 Kbytes, which means the hardware configuration of this sensor can be done in 7 seconds by using the low-speed transceiver. The remote hardware reconfiguration can be used to activate the sensor to capture and analyze image by the developed MIPS processor and to provide changes to pixels sensor operation based on the surrounding environment such as reconfigure the pixels sensor from video capturing to still image mode or change the capturing from black and white to color, if the RR-node supported with two different kind of pixels sensor.

The RR-node architecture is shown in Figure 2. The FPGA chip is including the soft-core processor; Pixels sensor and flash memory interfaces, and the JTAG controller. All other off-the-shelf components such as the CMOS pixels sensor, memory, solar unit, and node's batteries are placed along with the FPGA Spartan 3 chip on RR-node's PCB board.

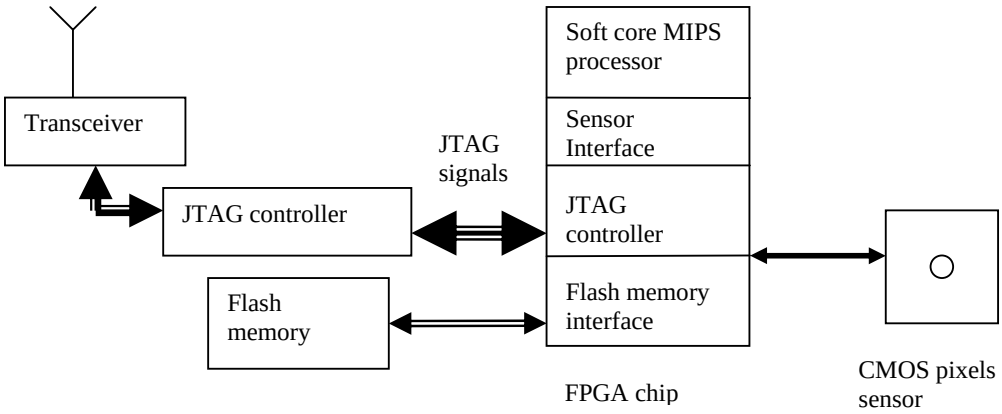

Figure 2RR-node architecture

4.CONCLUSIONS

The RR-node is designed to support remote hardware reconfiguration in addition to remote software reprogramming to provide a full flexible node design. Such node can provide a remote design modification that support nodes design adjusting to the surrounding applications. The use of partial reconfiguration and file compression techniques in addition to the use of tiny solar unit to node's battery charging can overcome the high power consumption generated by the use of FPGA chip in the proposed sensor node. The evaluation for hardware modification to some of components used in RR-node design has shown that some node features can be upgraded in acceptable amount of time even when a slow wireless transceiver is used.

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